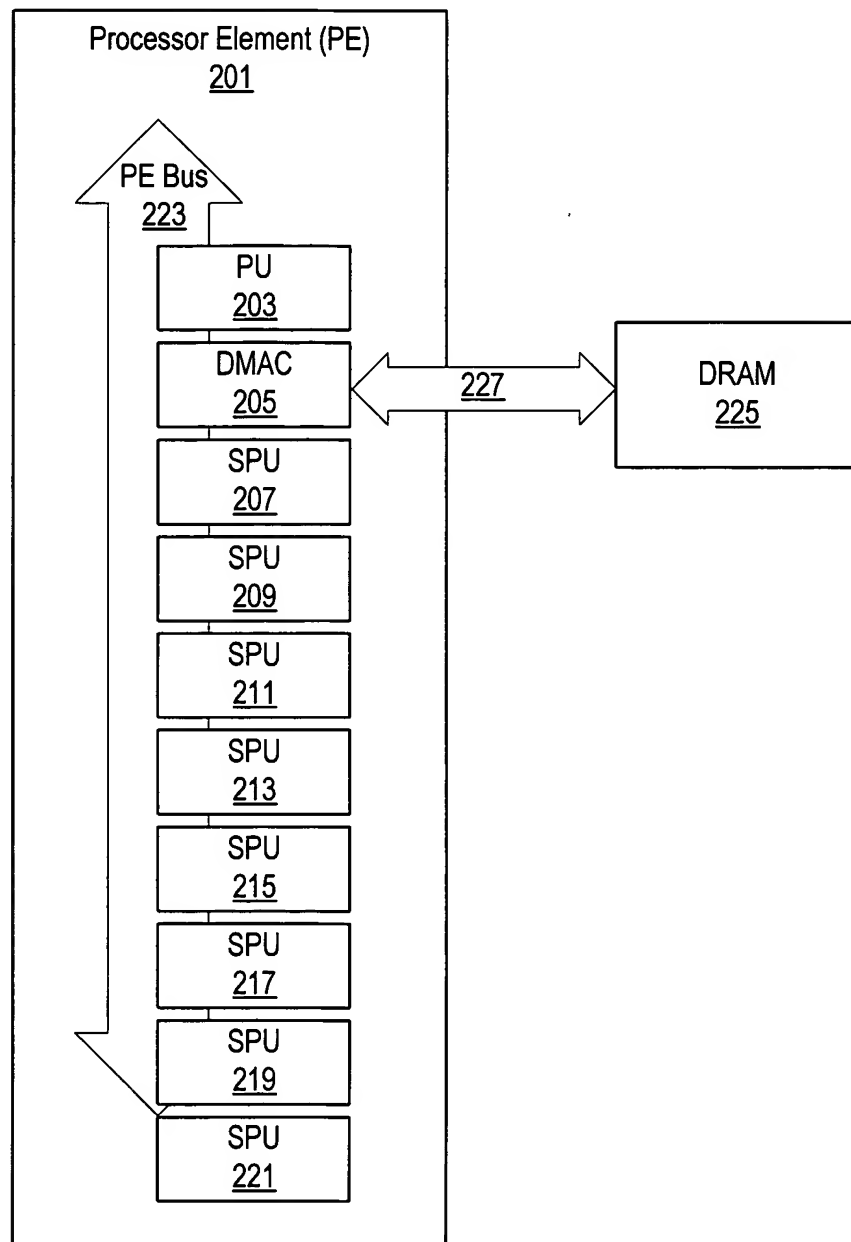
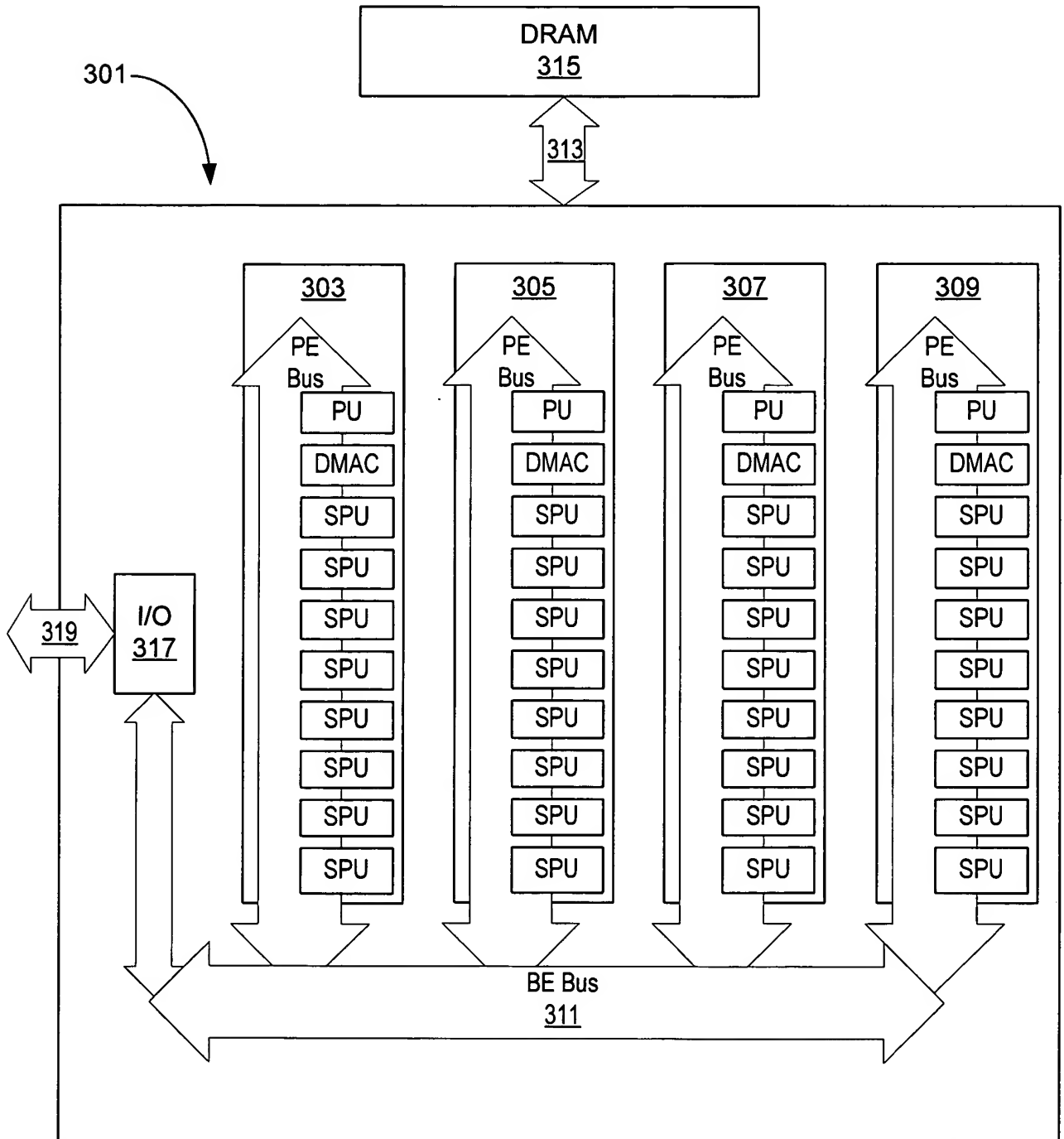
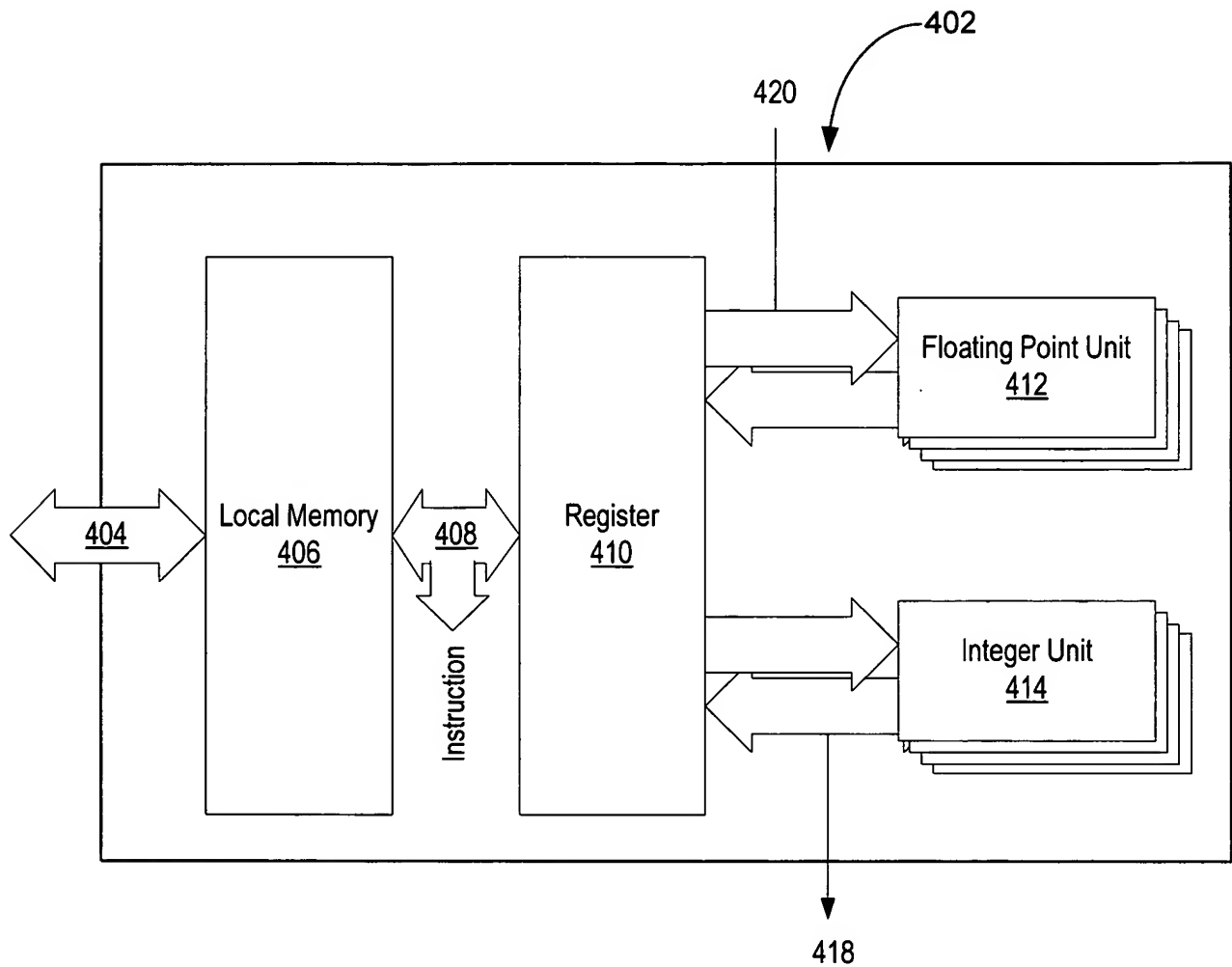
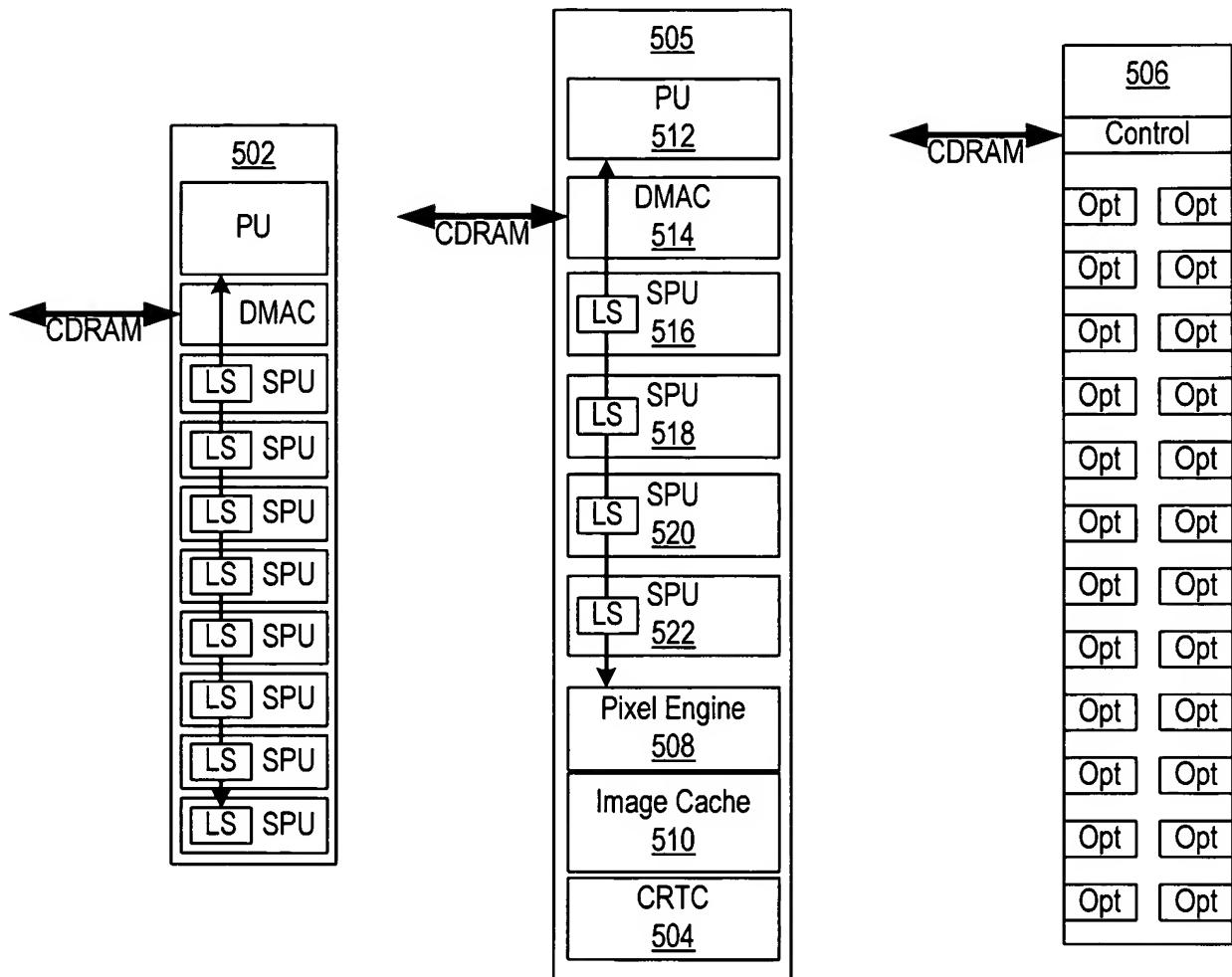
**Figure 1**

**Figure 2**

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**Figure 3**

**Figure 4**

**Figure 5**

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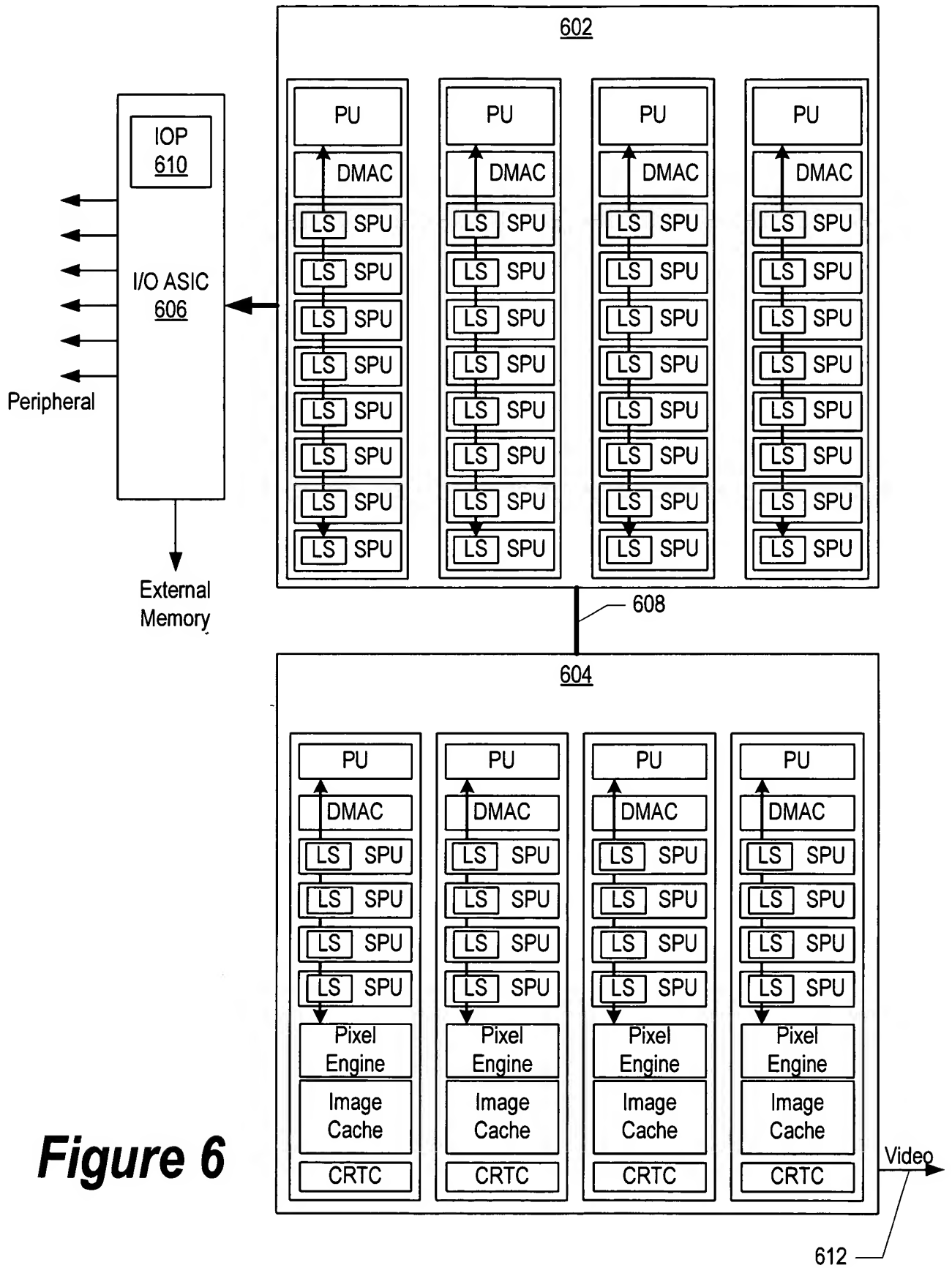
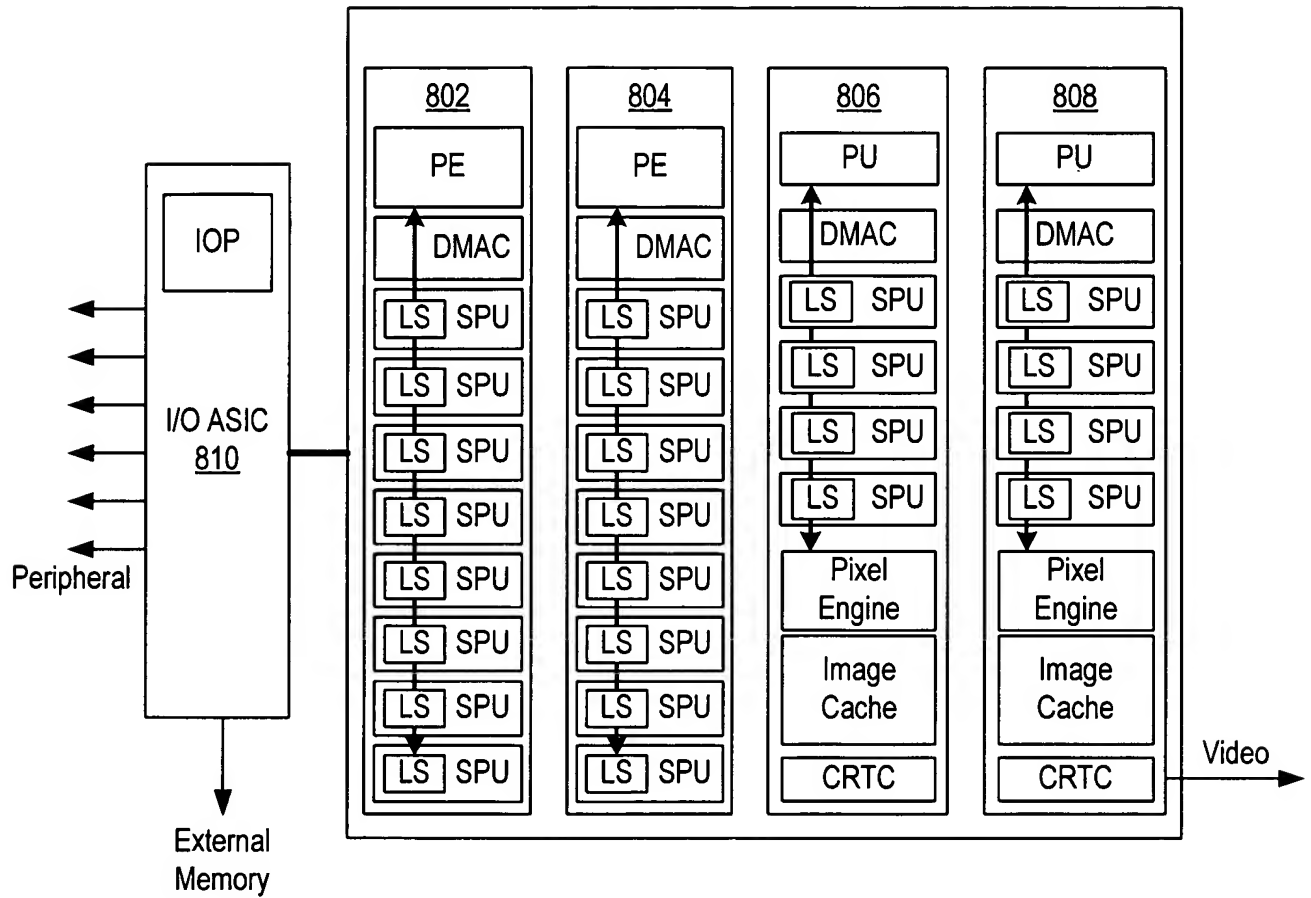
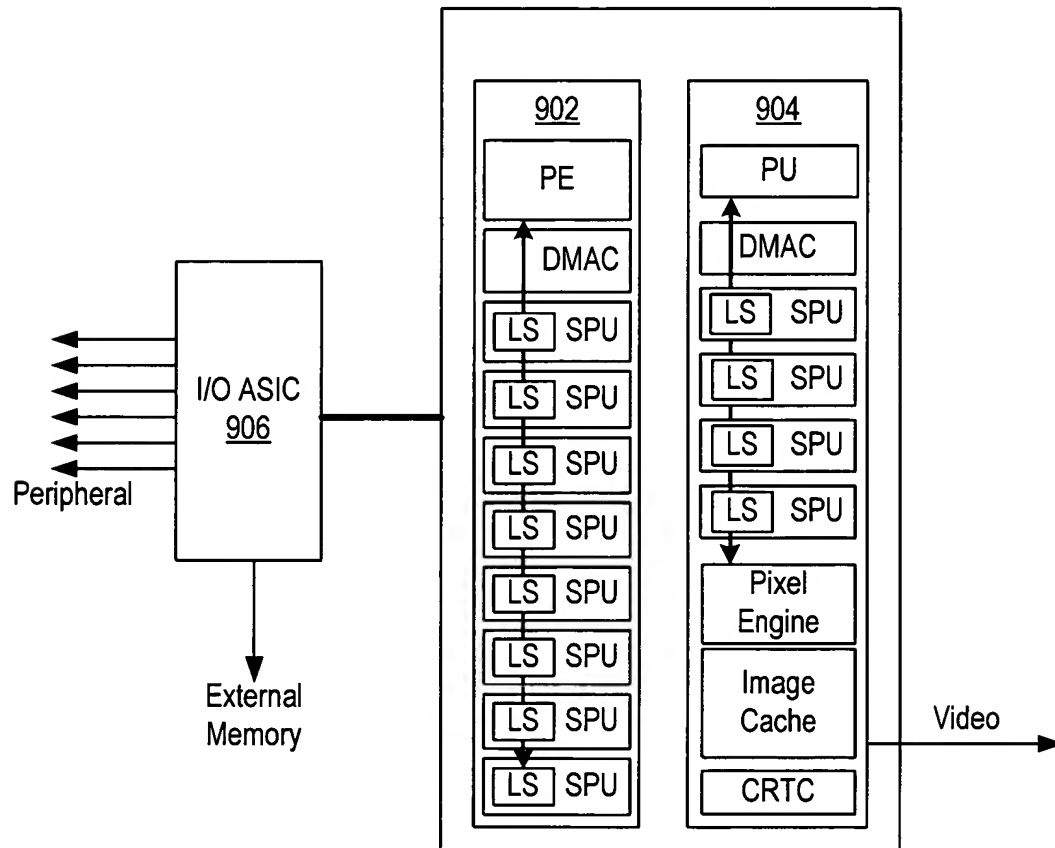
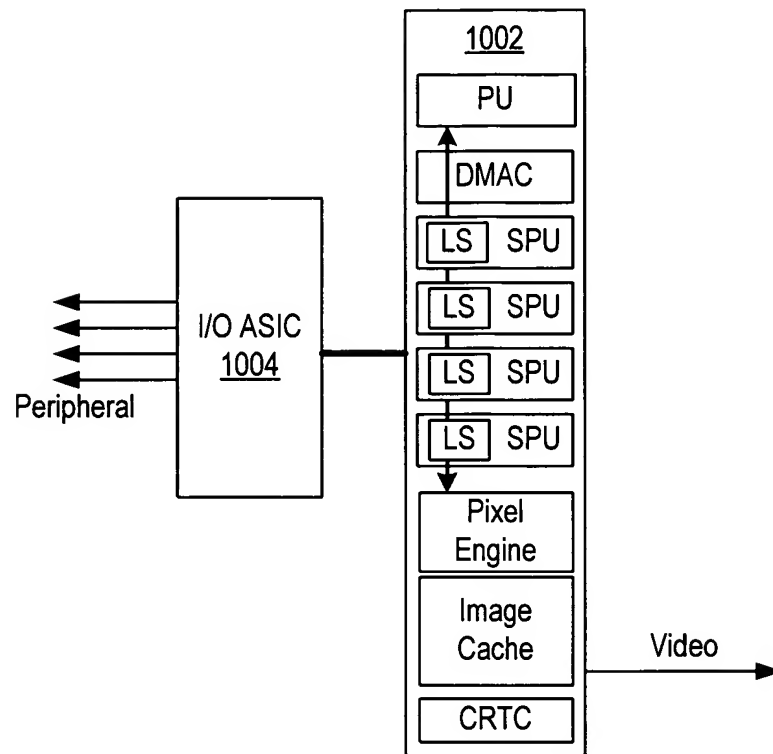
**Figure 6**

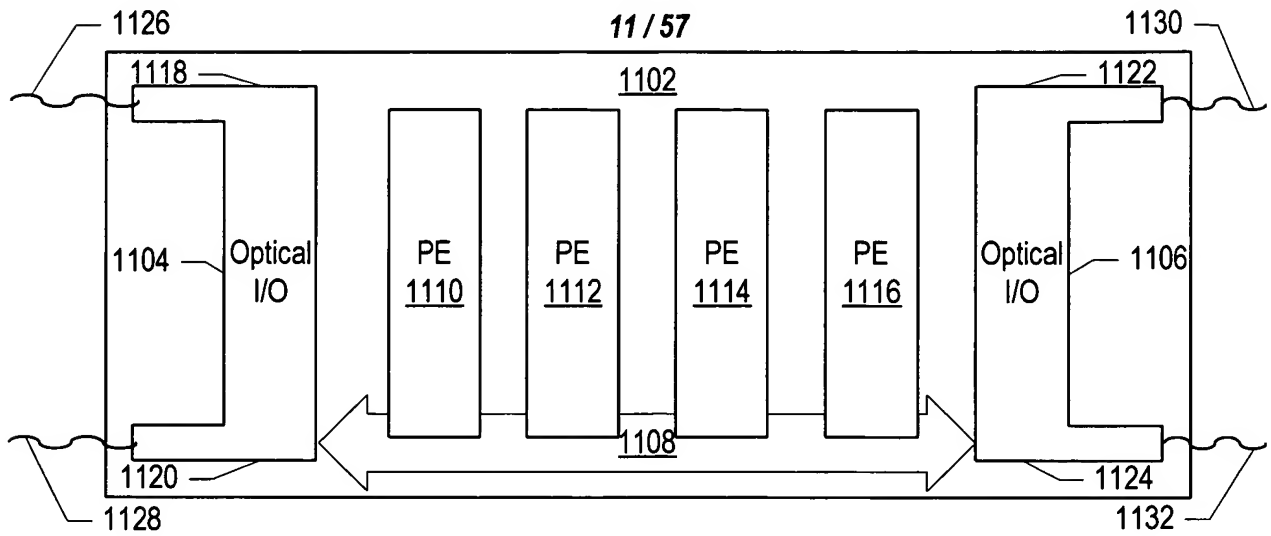
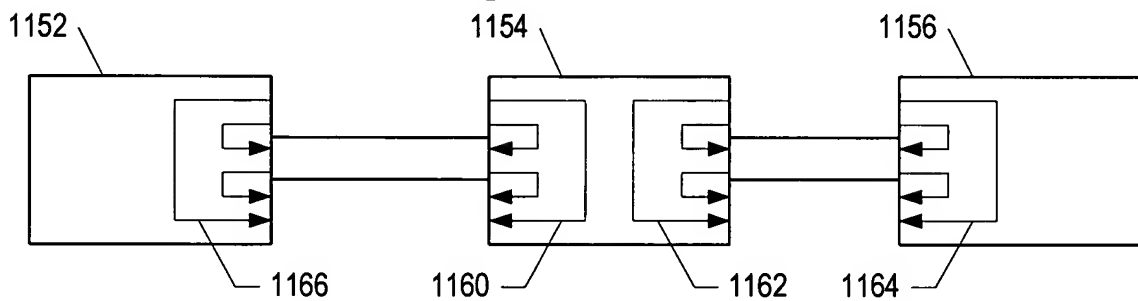
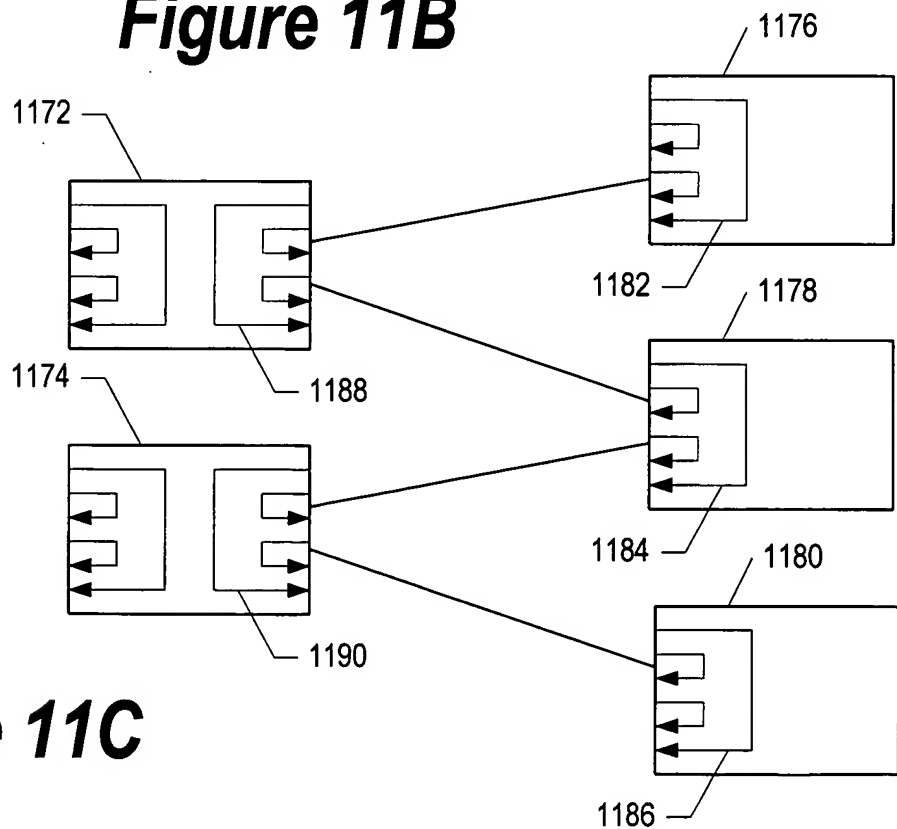


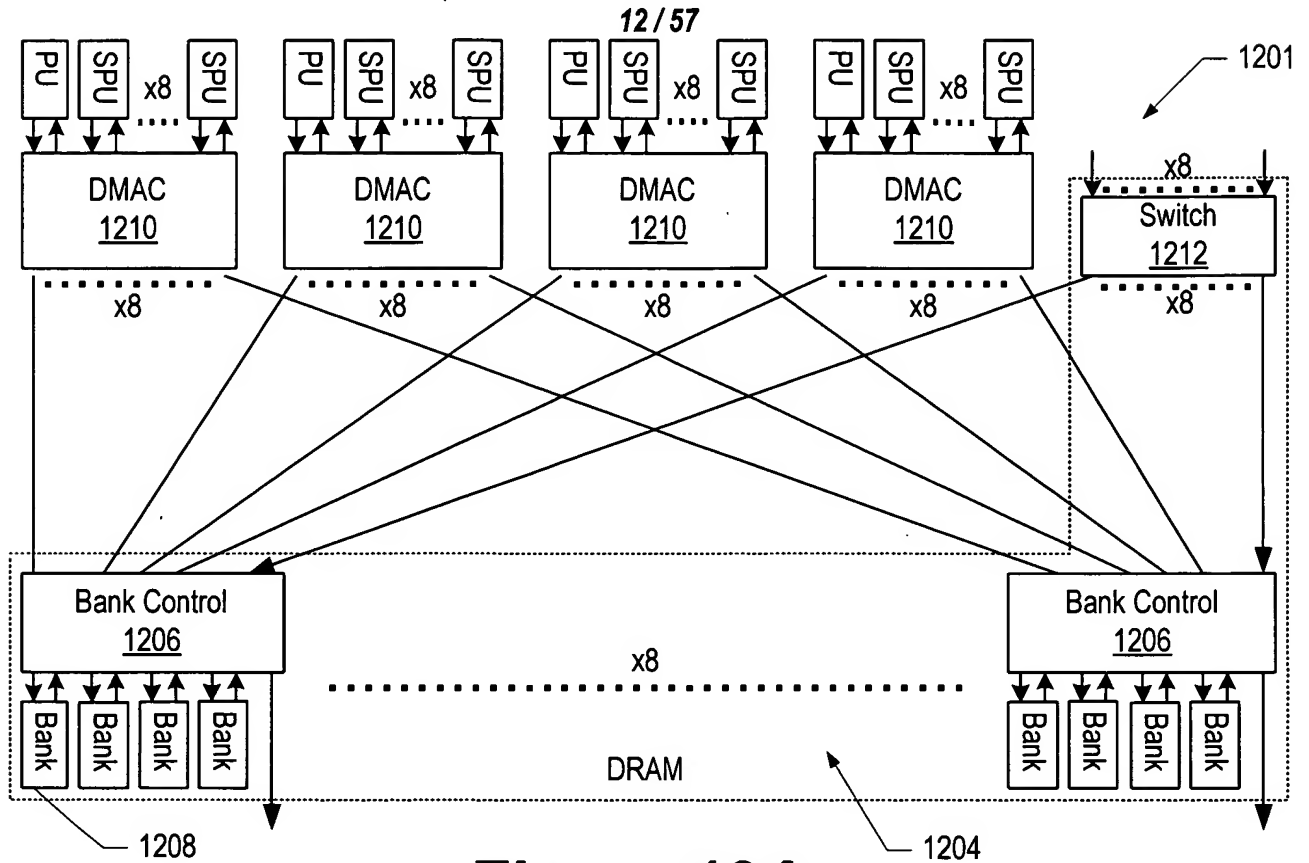
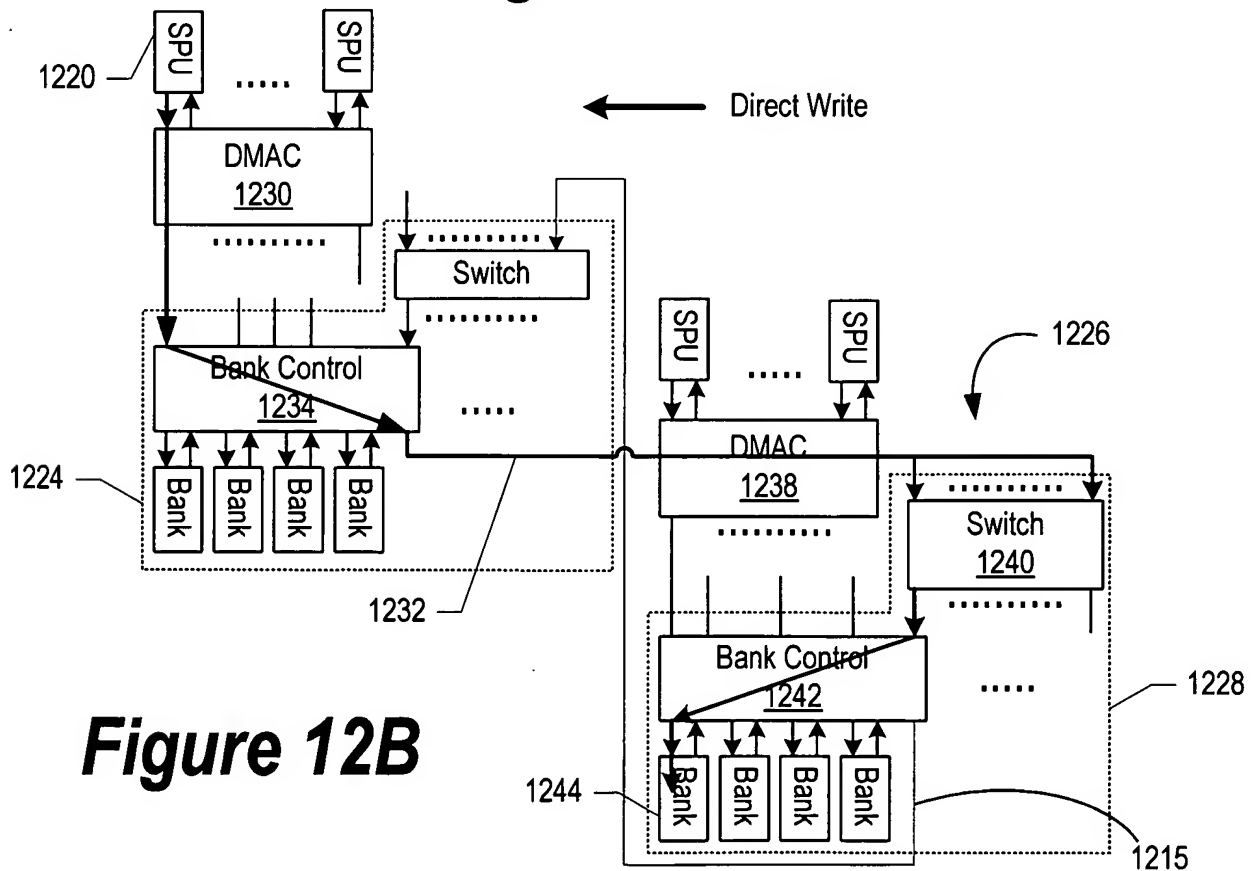
Figure 7

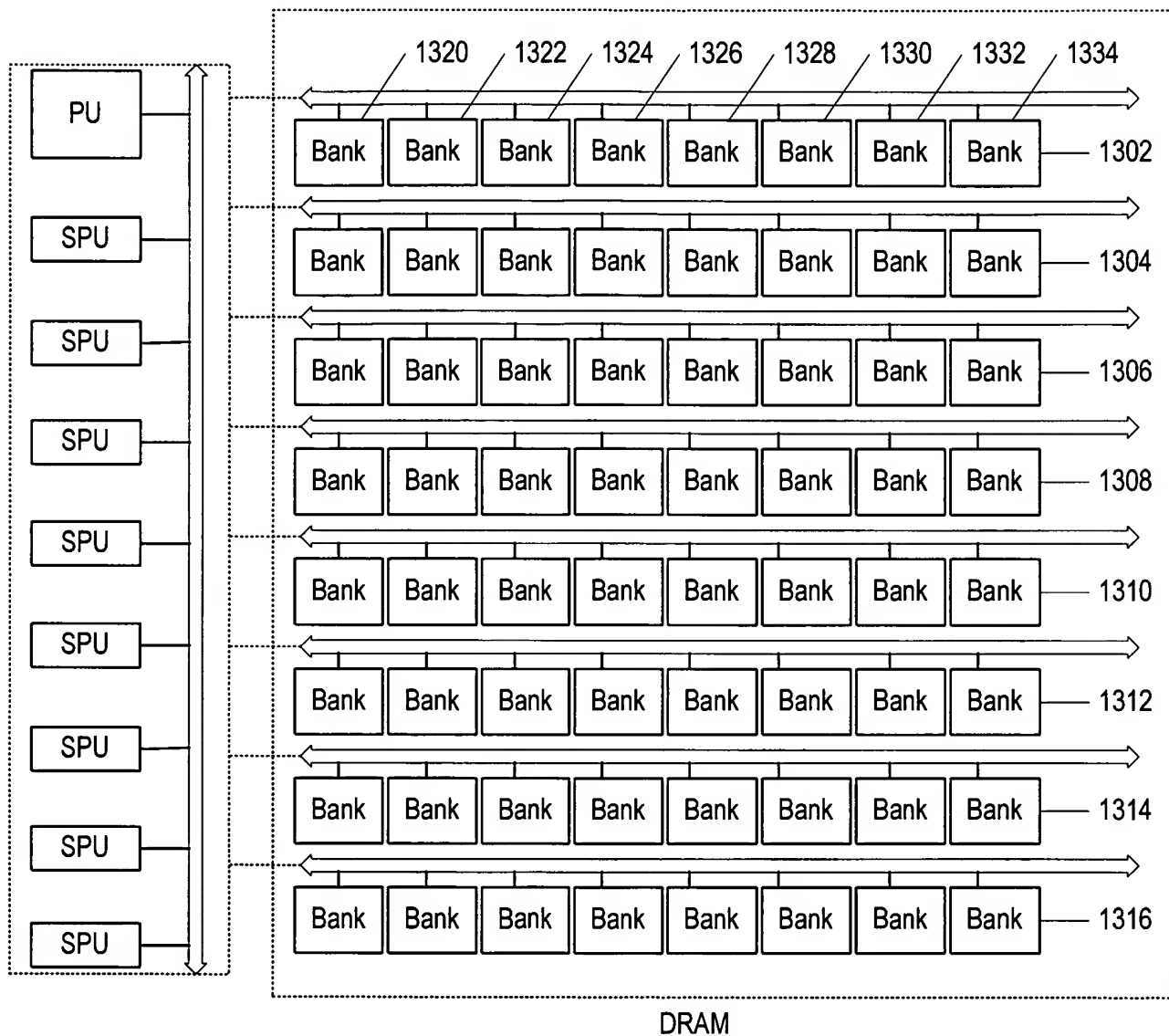
**Figure 8**

**Figure 9**

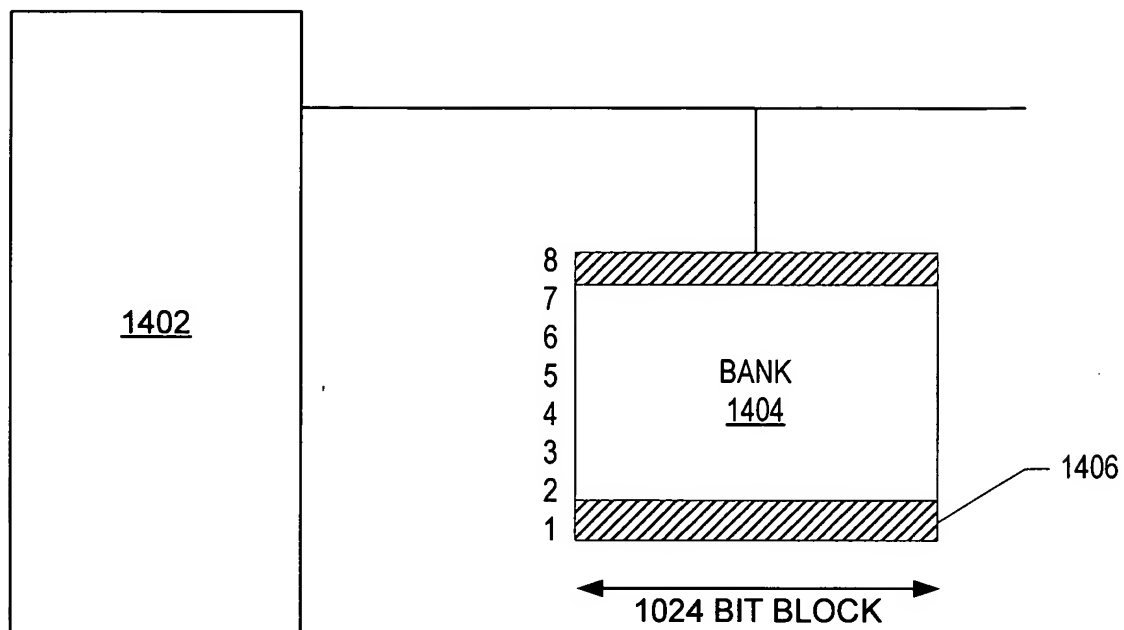
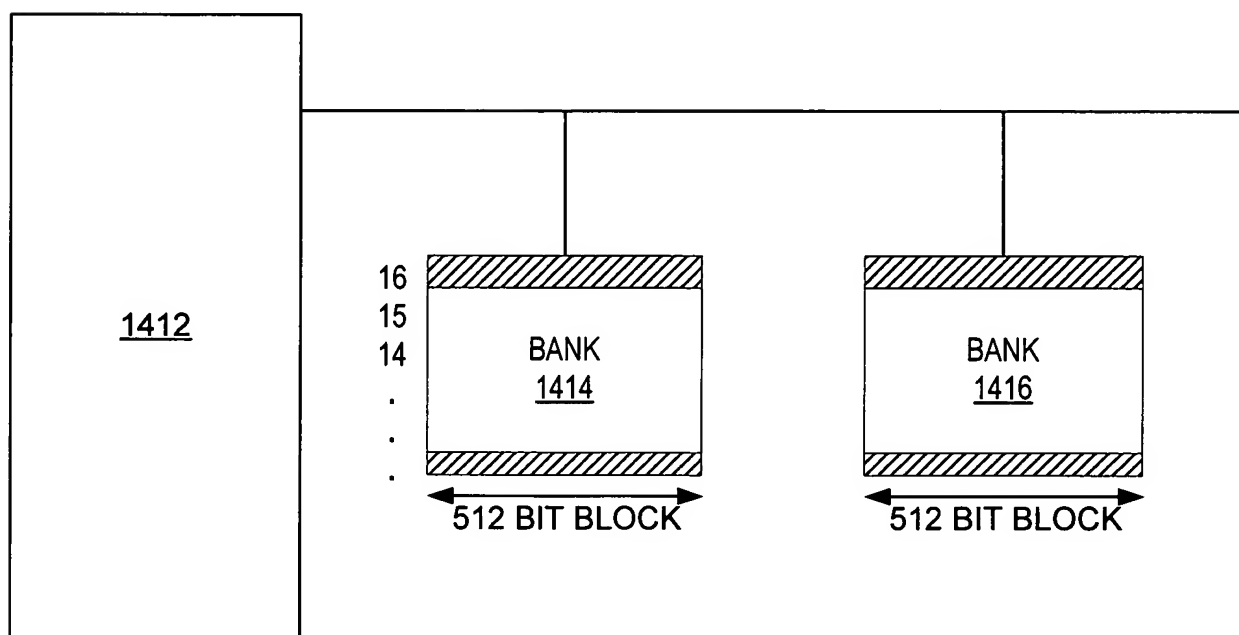
**Figure 10**

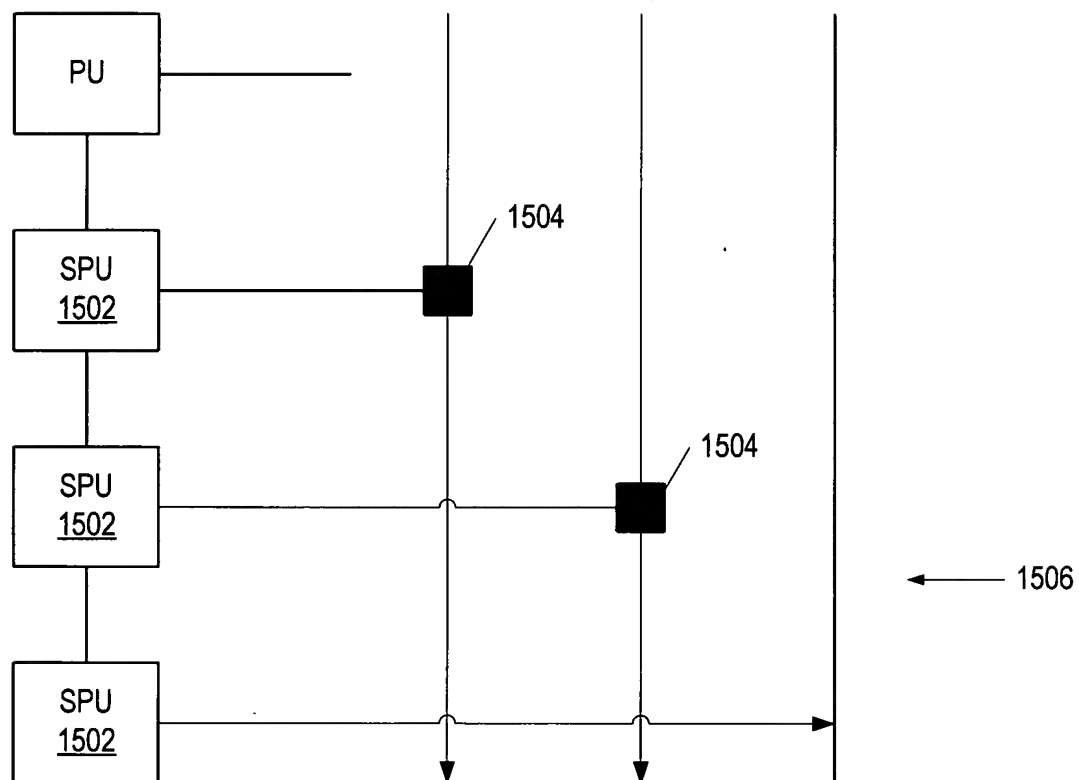
**Figure 11A****Figure 11B****Figure 11C**

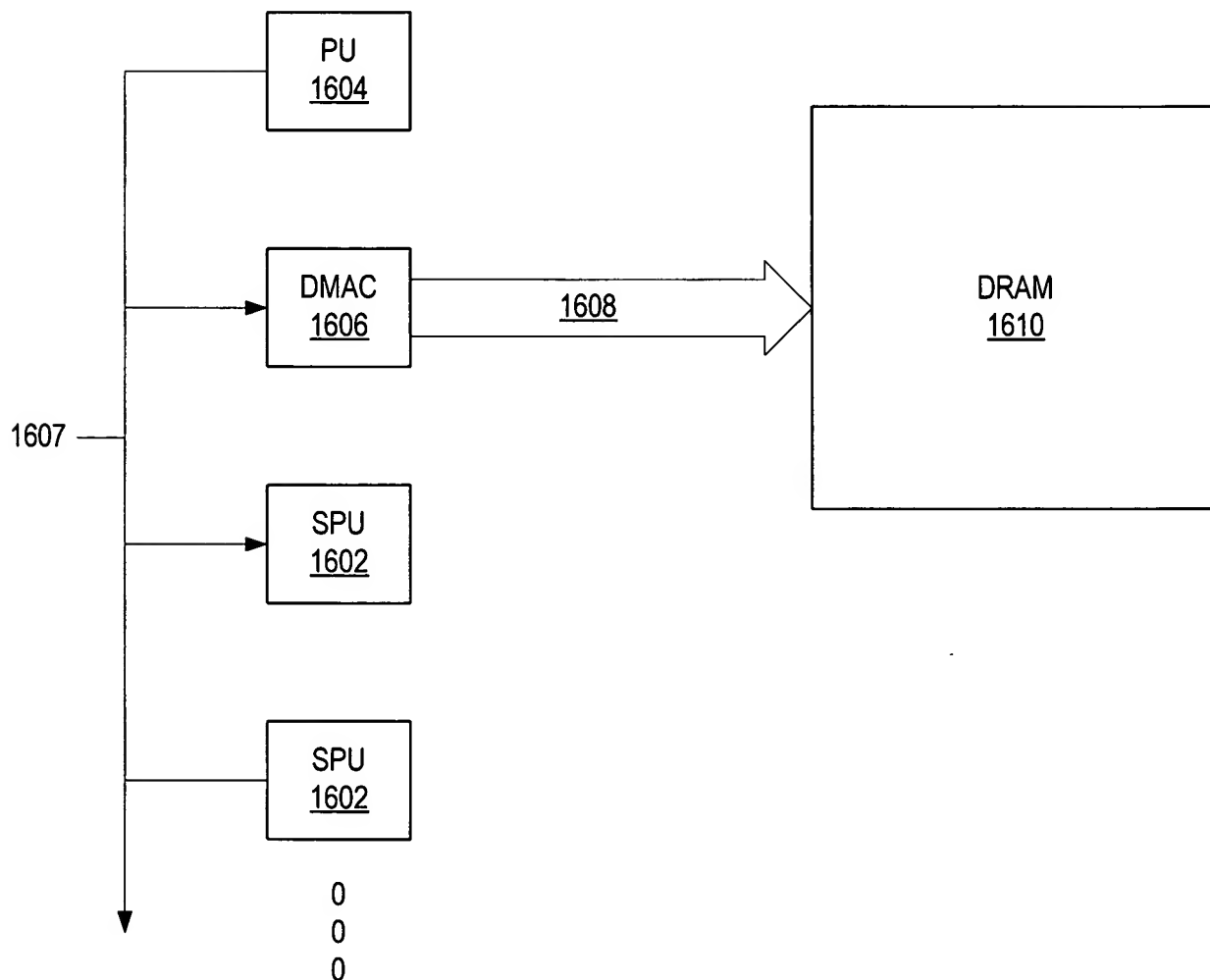
**Figure 12A****Figure 12B**

**Figure 13**

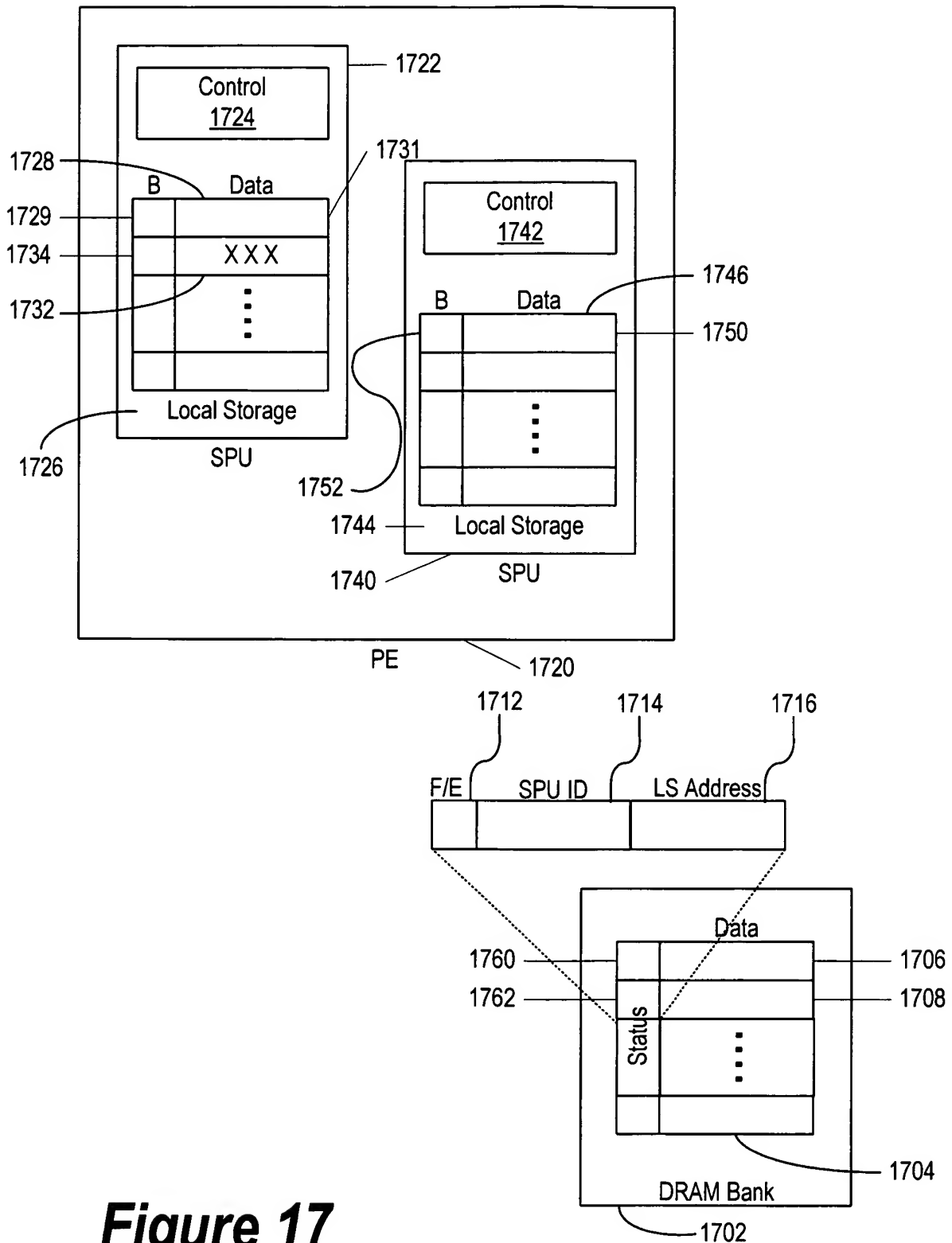
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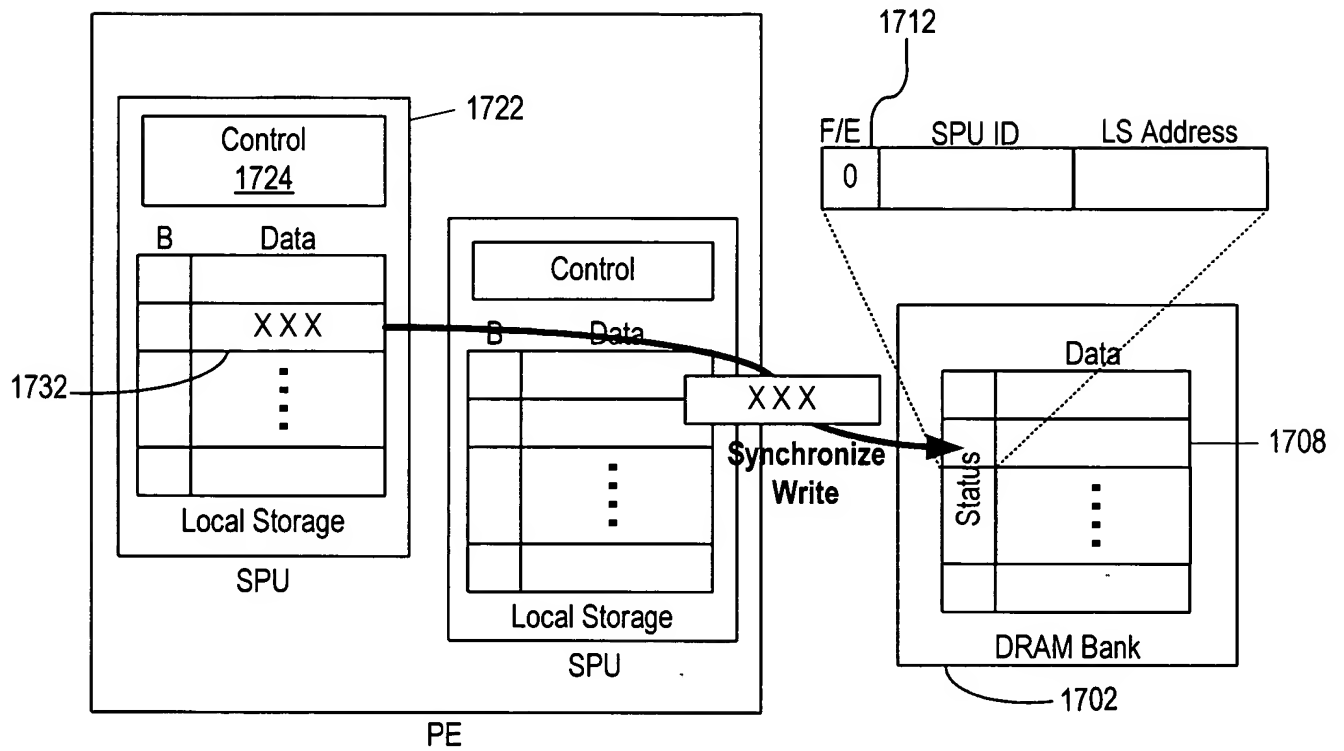
**Figure 14A****Figure 14B**

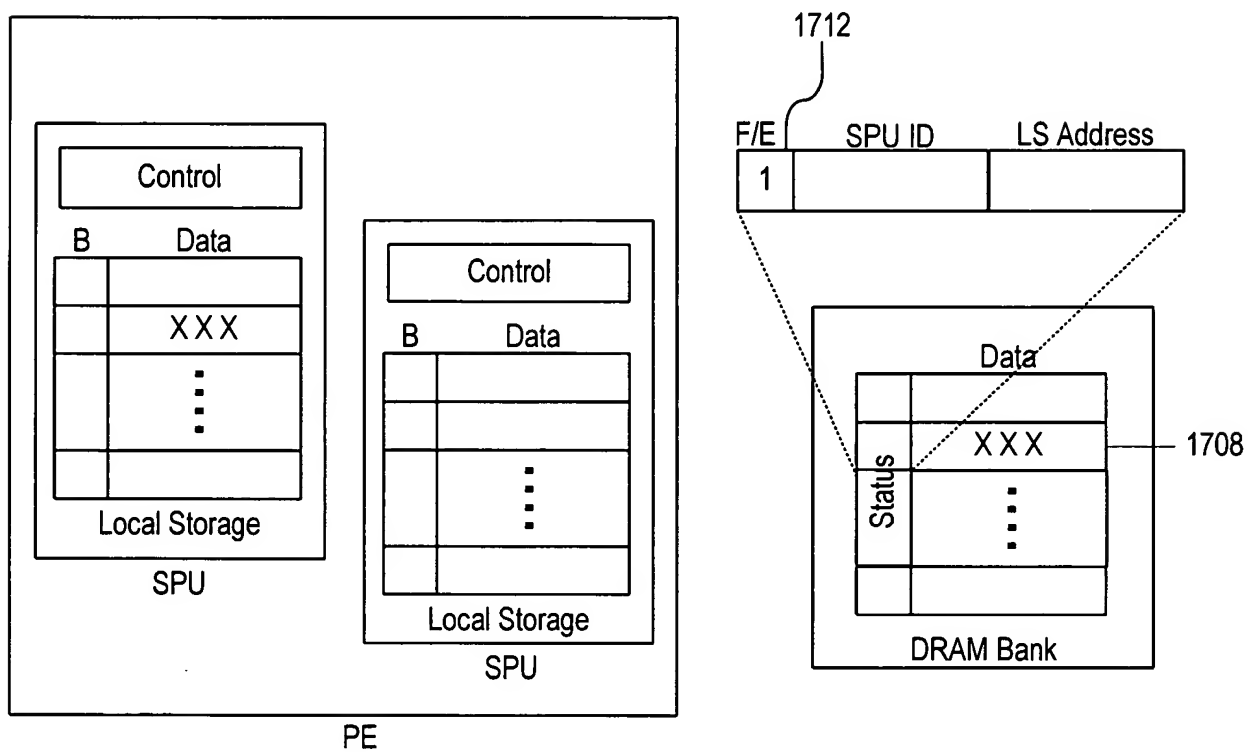
**Figure 15**

**Figure 16**

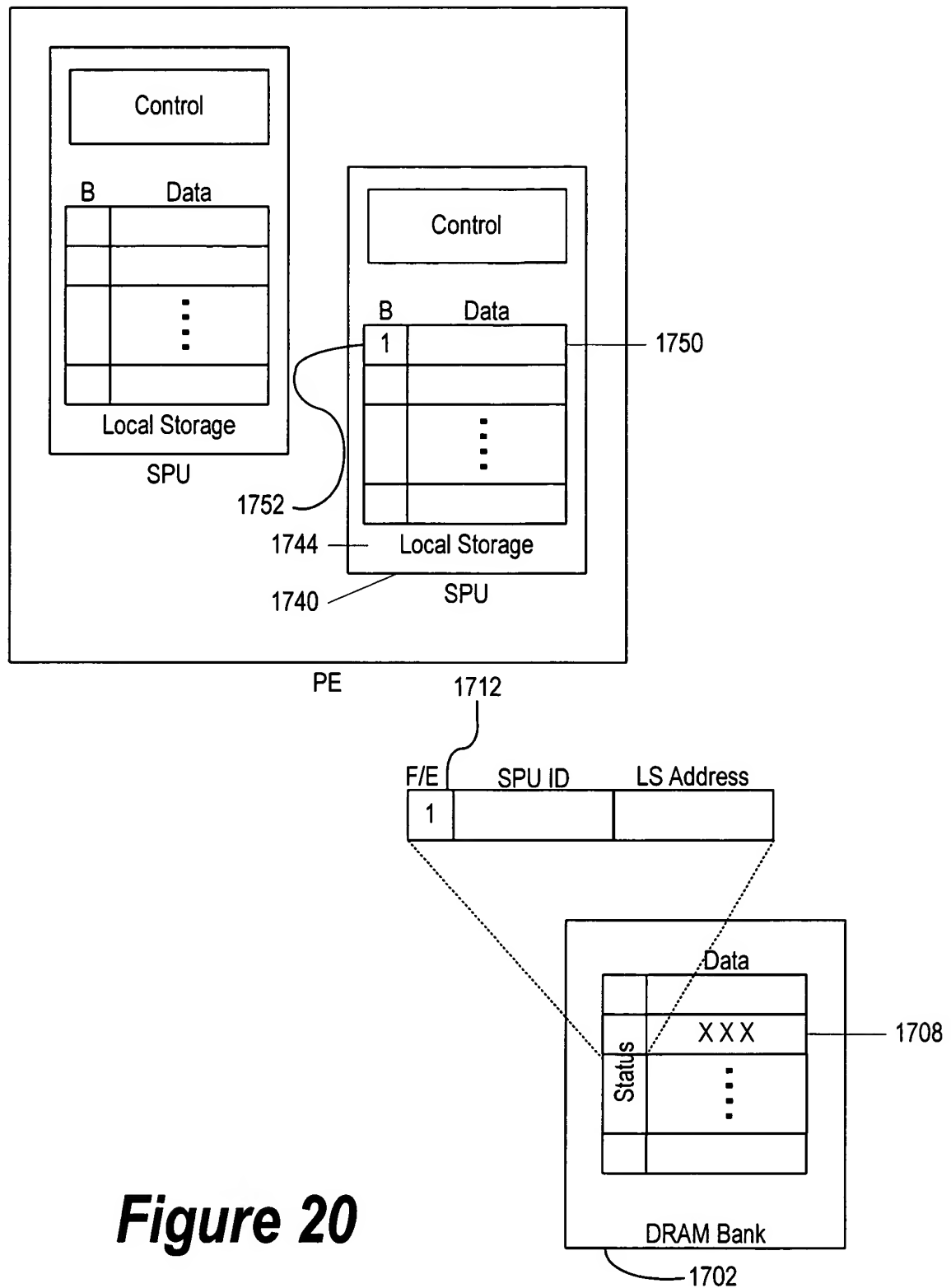
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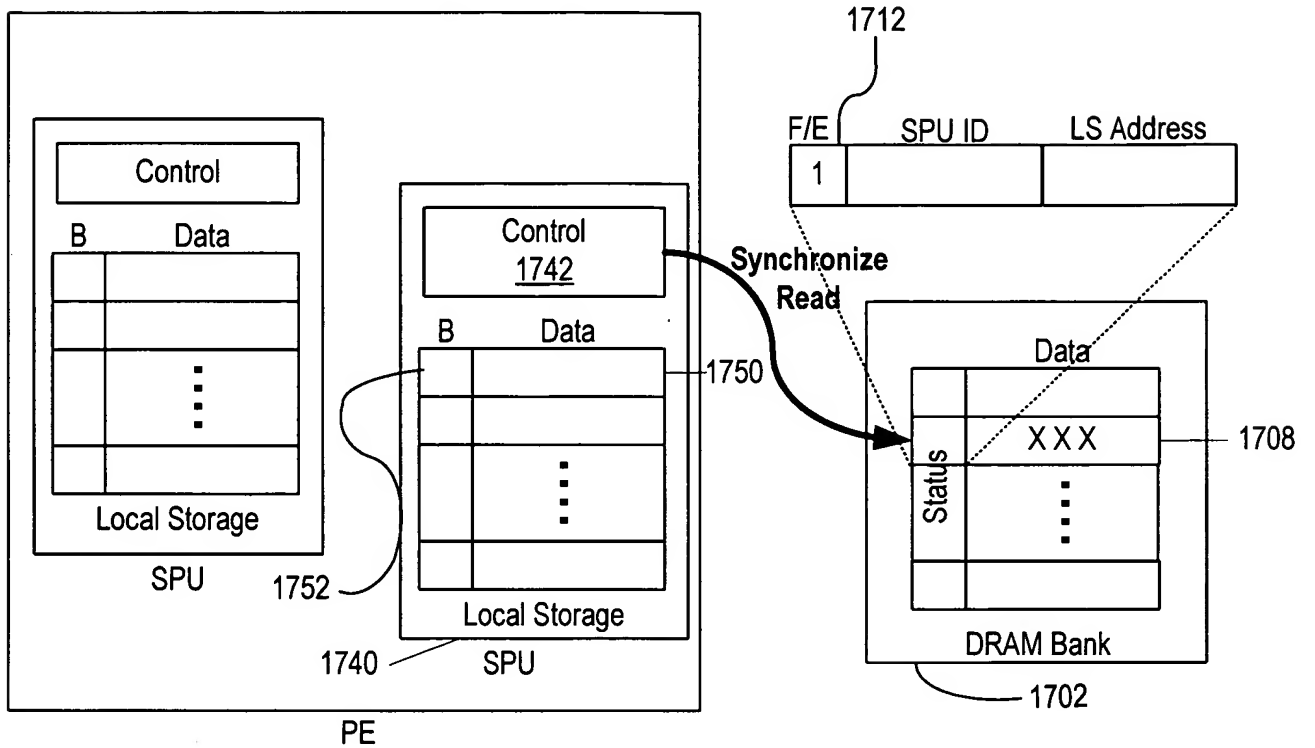
**Figure 17**

**Figure 18**

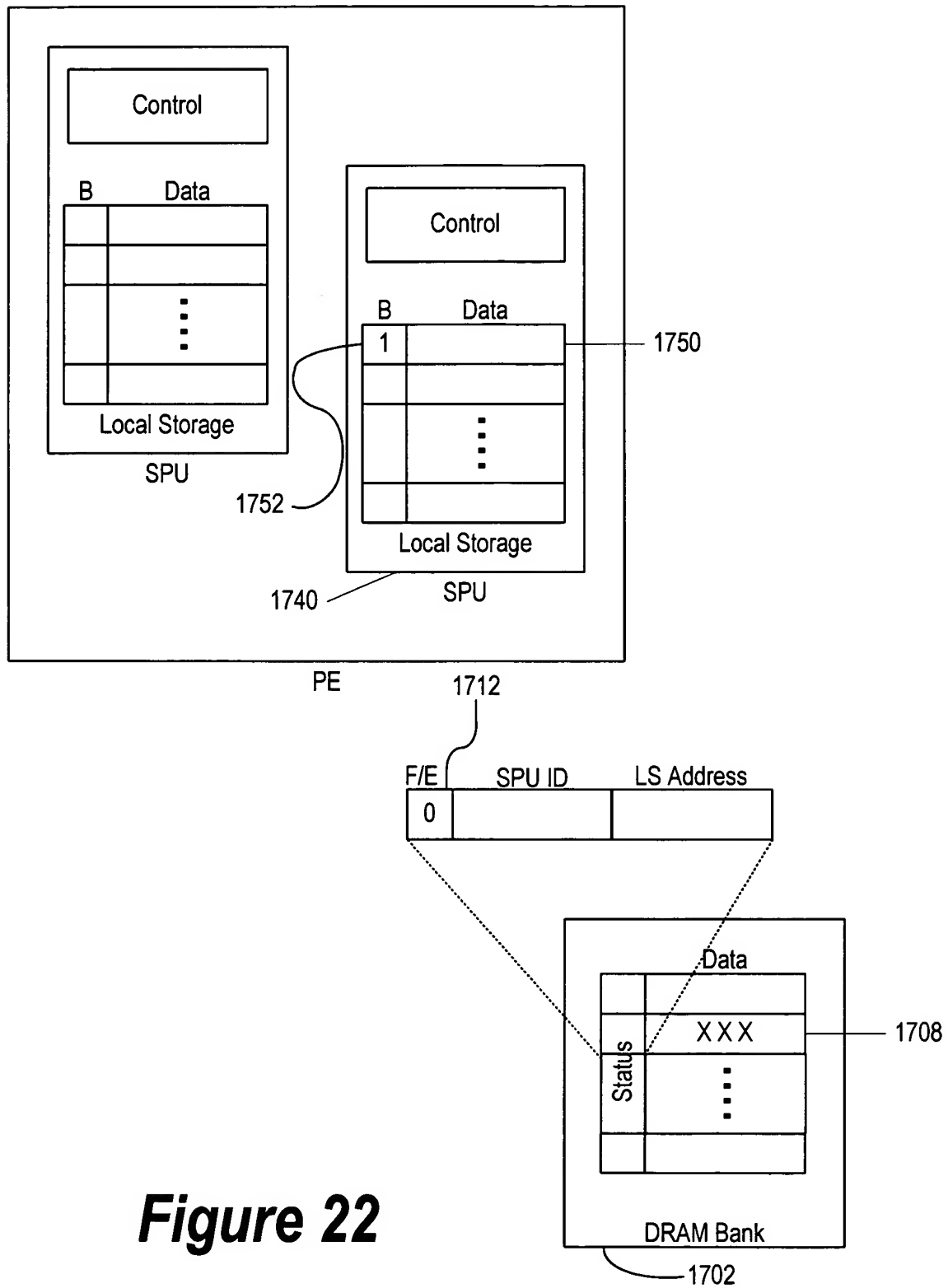
**Figure 19**

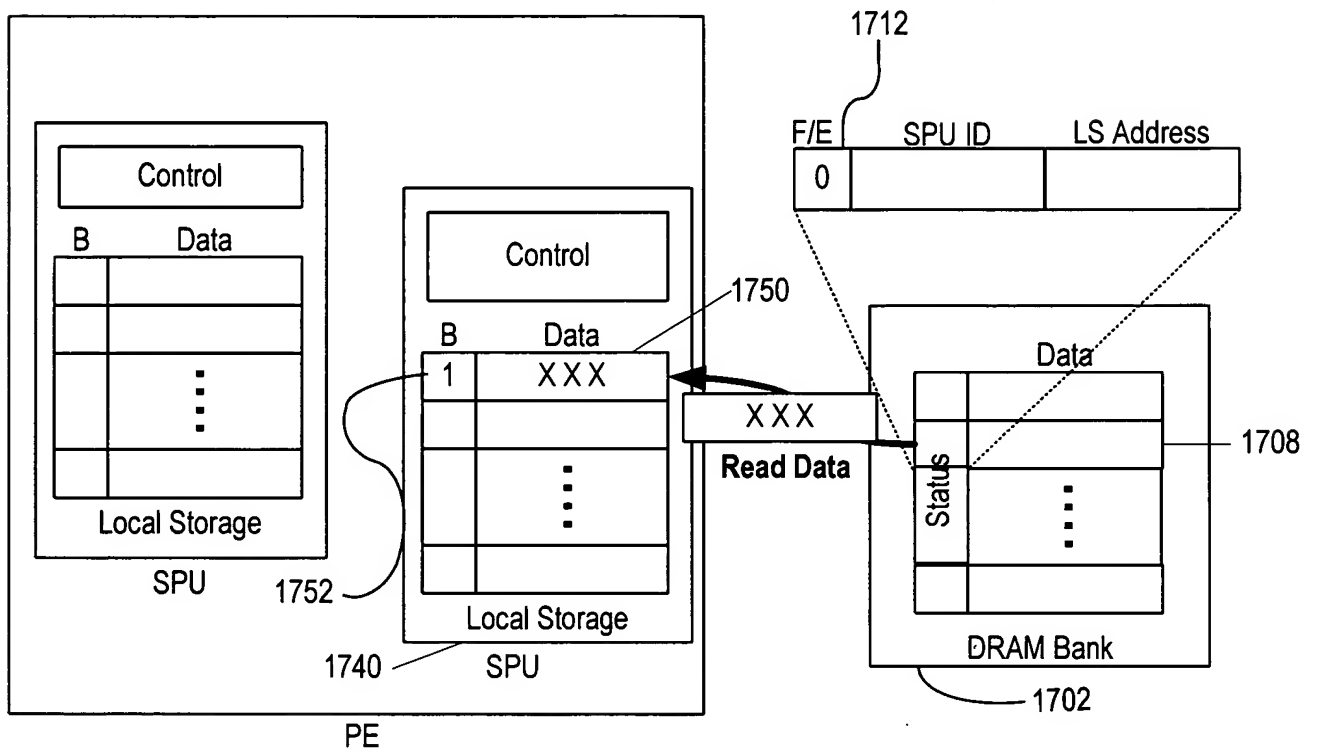
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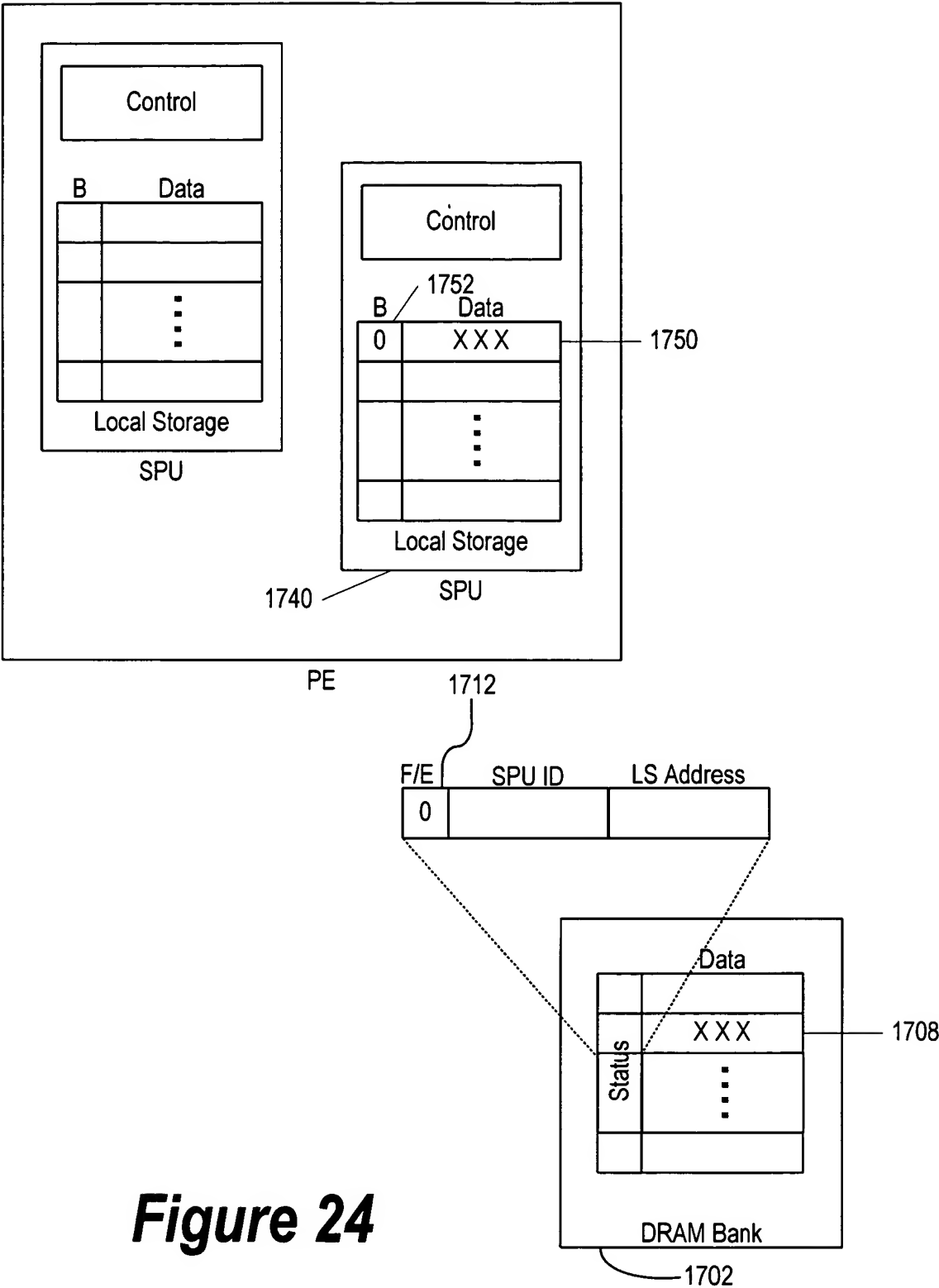
**Figure 20**

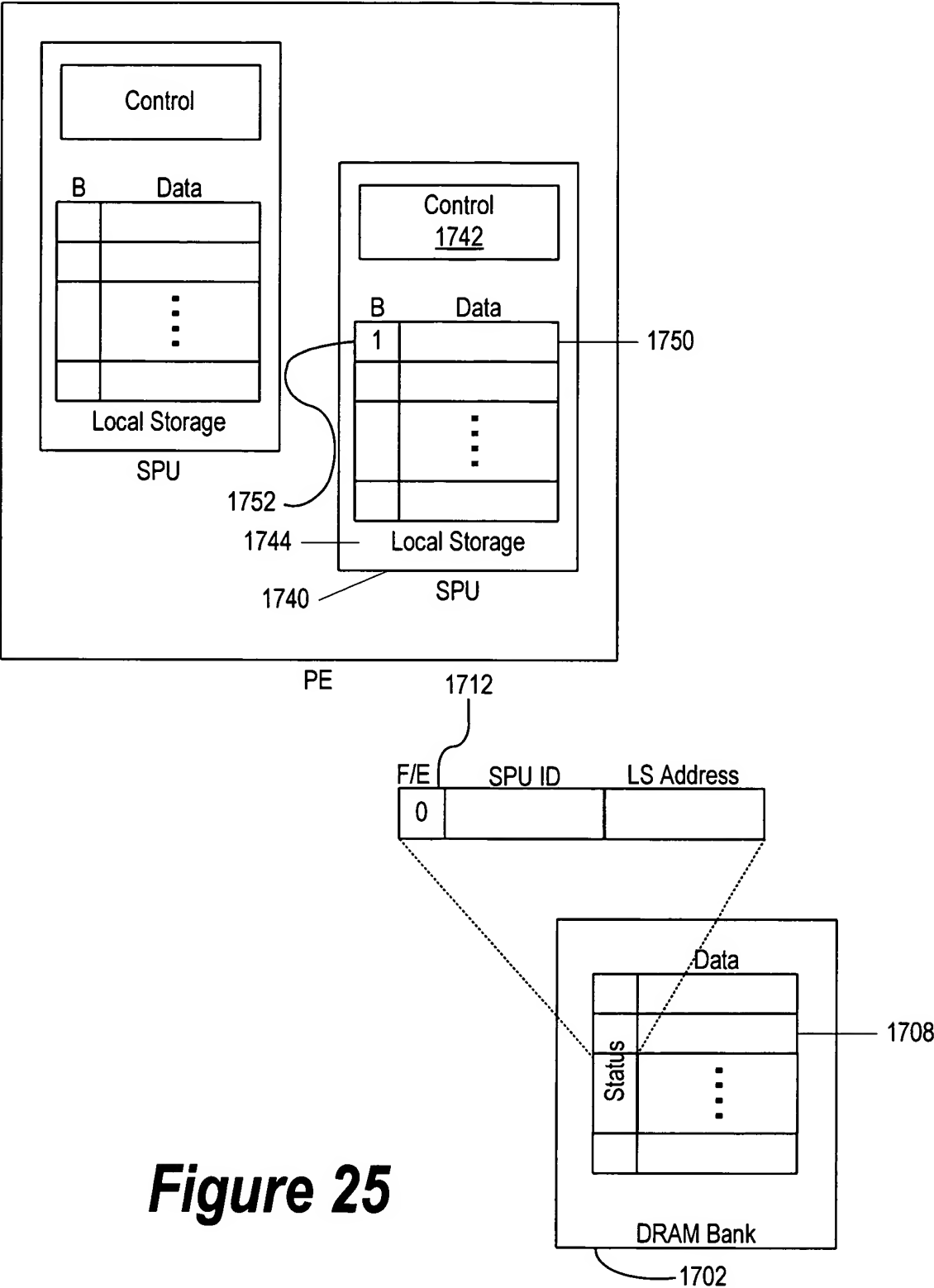
**Figure 21**

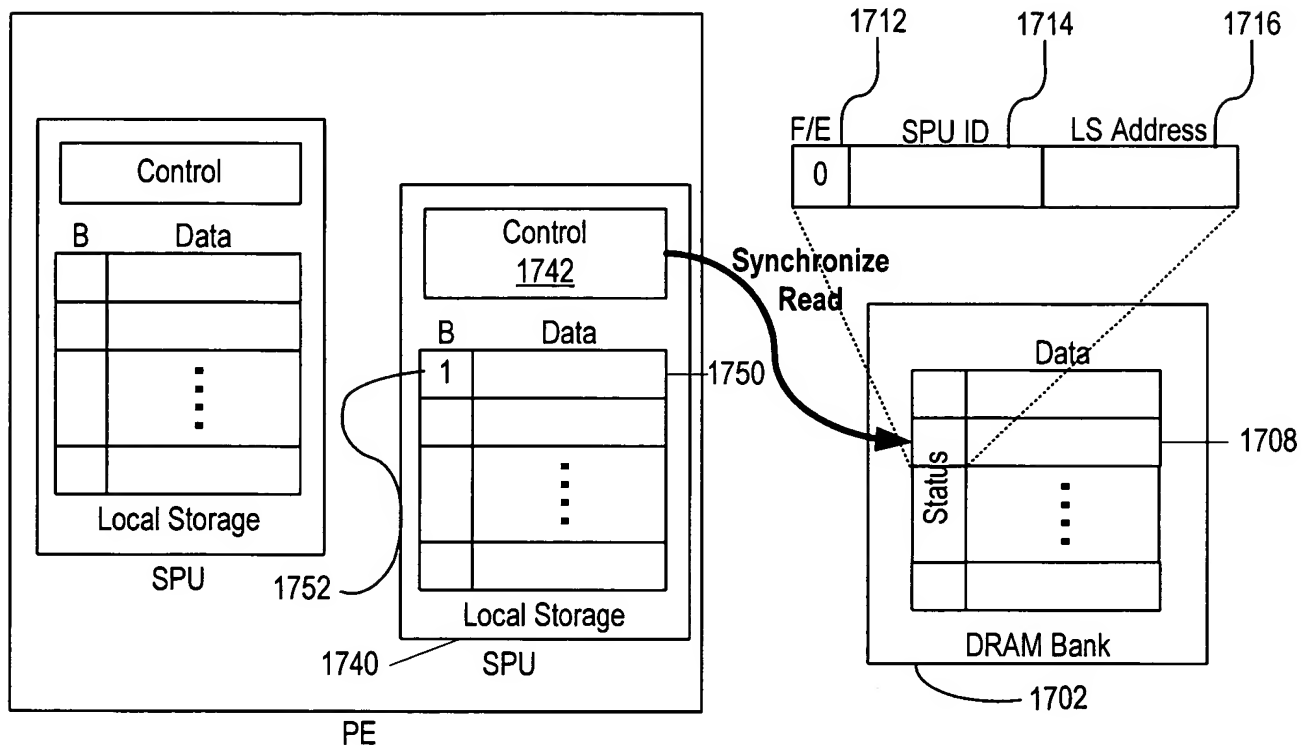
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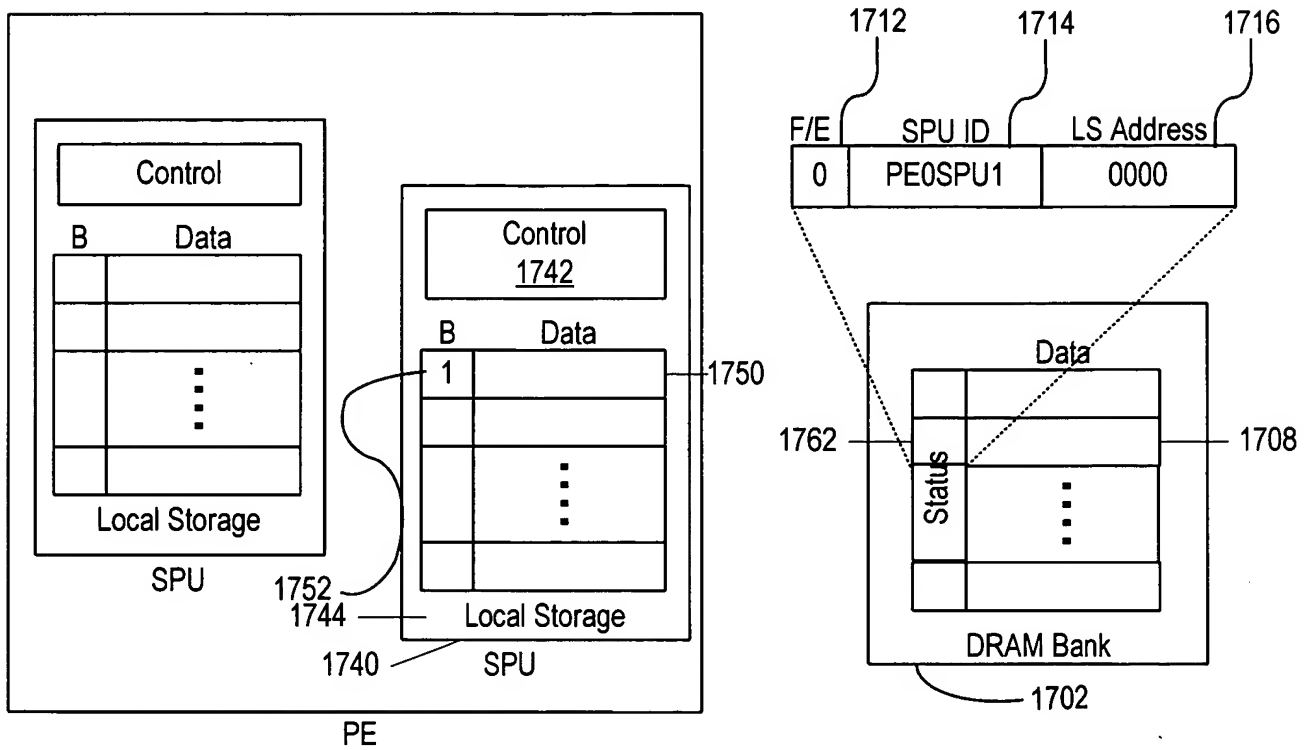
**Figure 22**

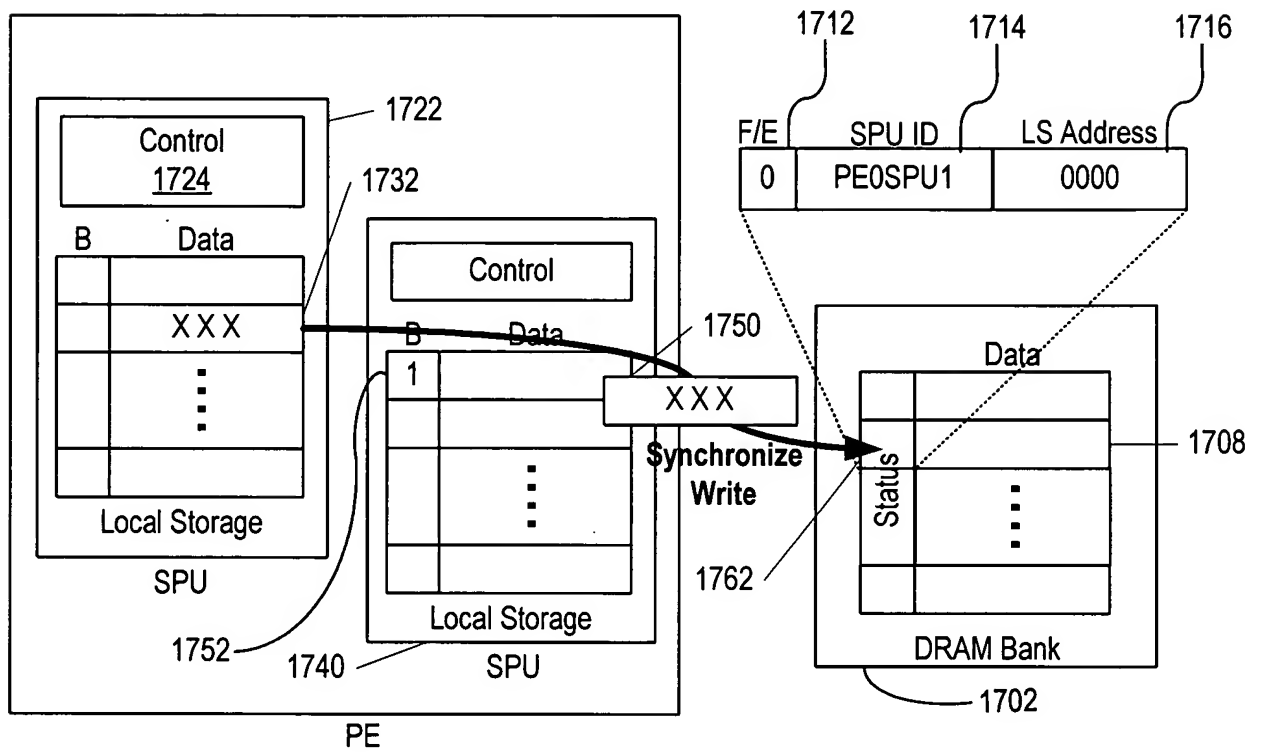
**Figure 23**

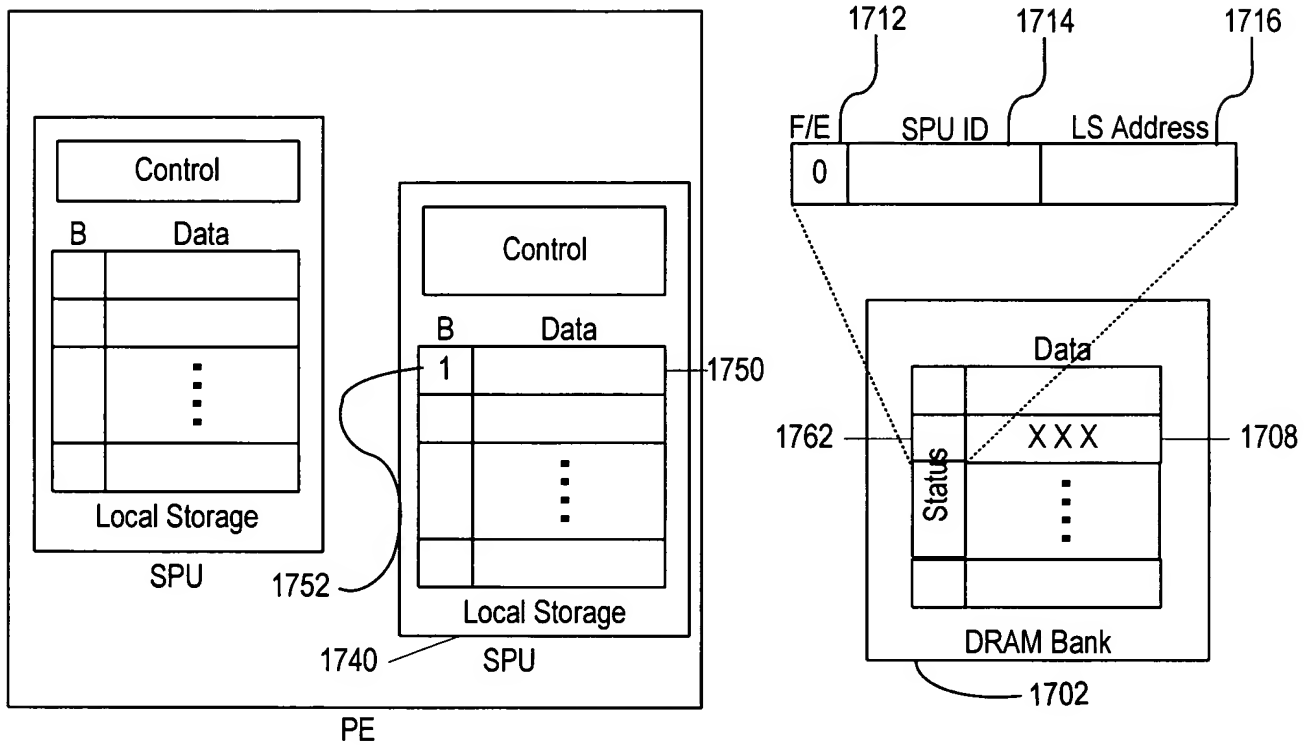


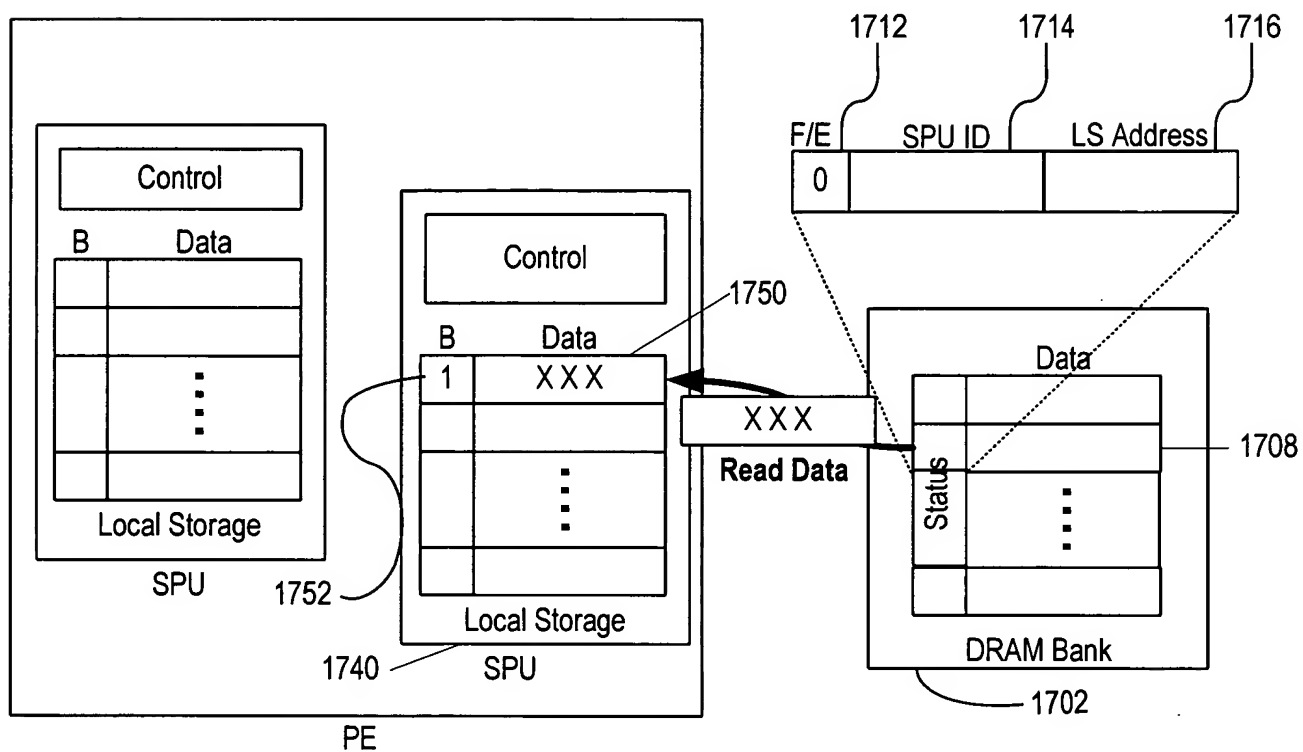


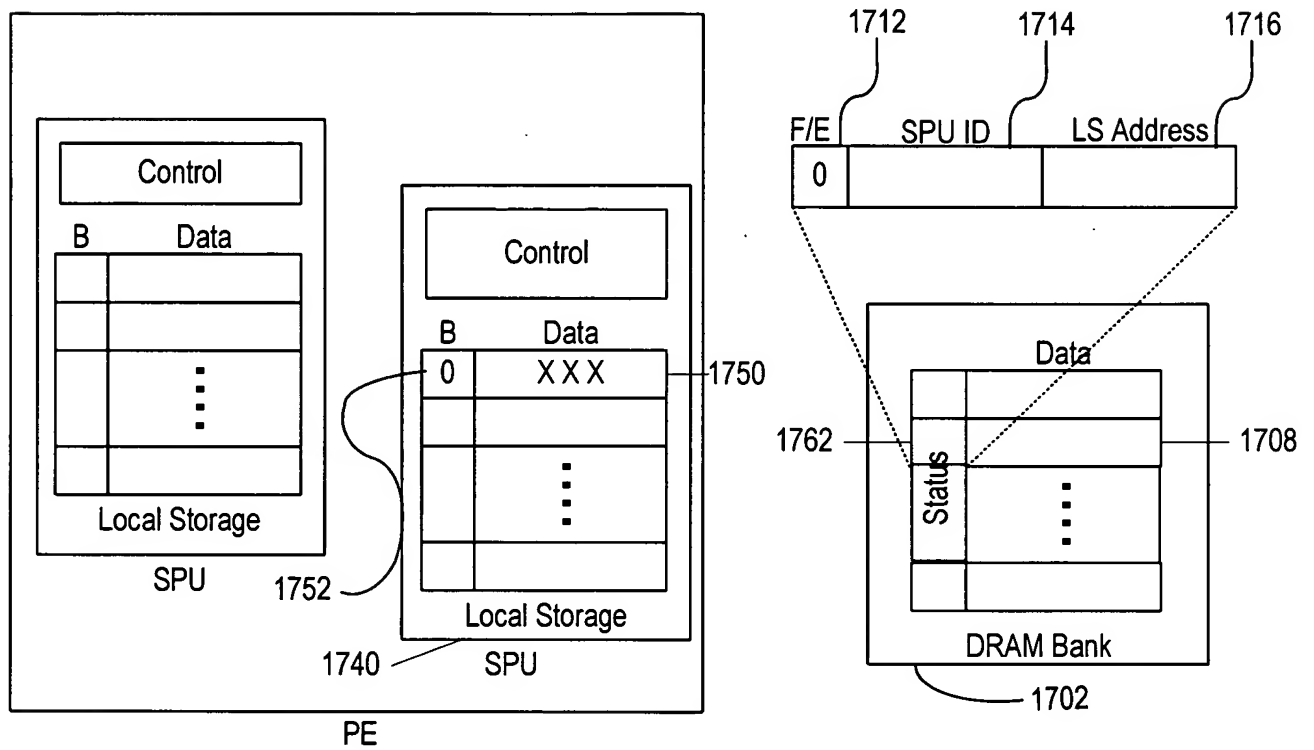
**Figure 26**

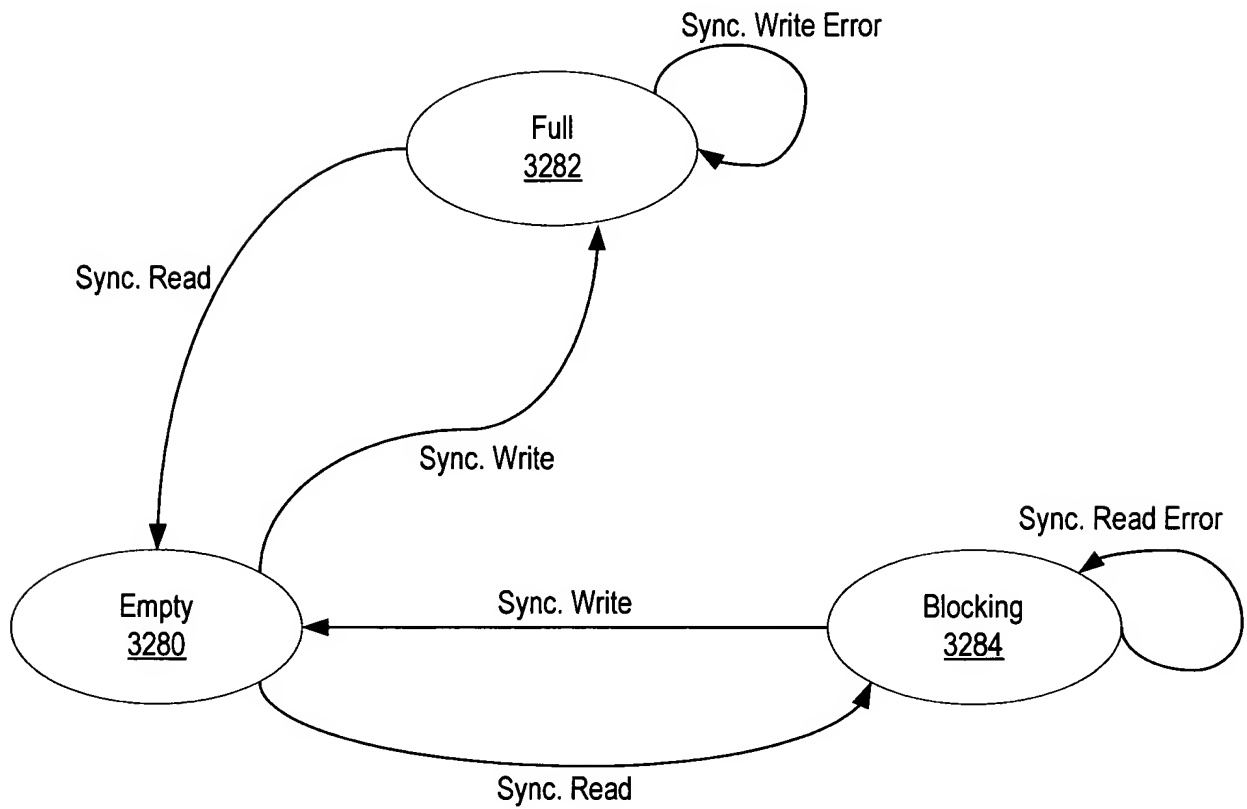
**Figure 27**

**Figure 28**

**Figure 29**

**Figure 30**

**Figure 31**

**Figure 32**

Key Control Table

3302

3304 — ID			3306	3308
0	SPU Key	Key Mask		
1	SPU Key	Key Mask		
2	SPU Key	Key Mask		
		⋮		
7	SPU Key	Key Mask		

Figure 33

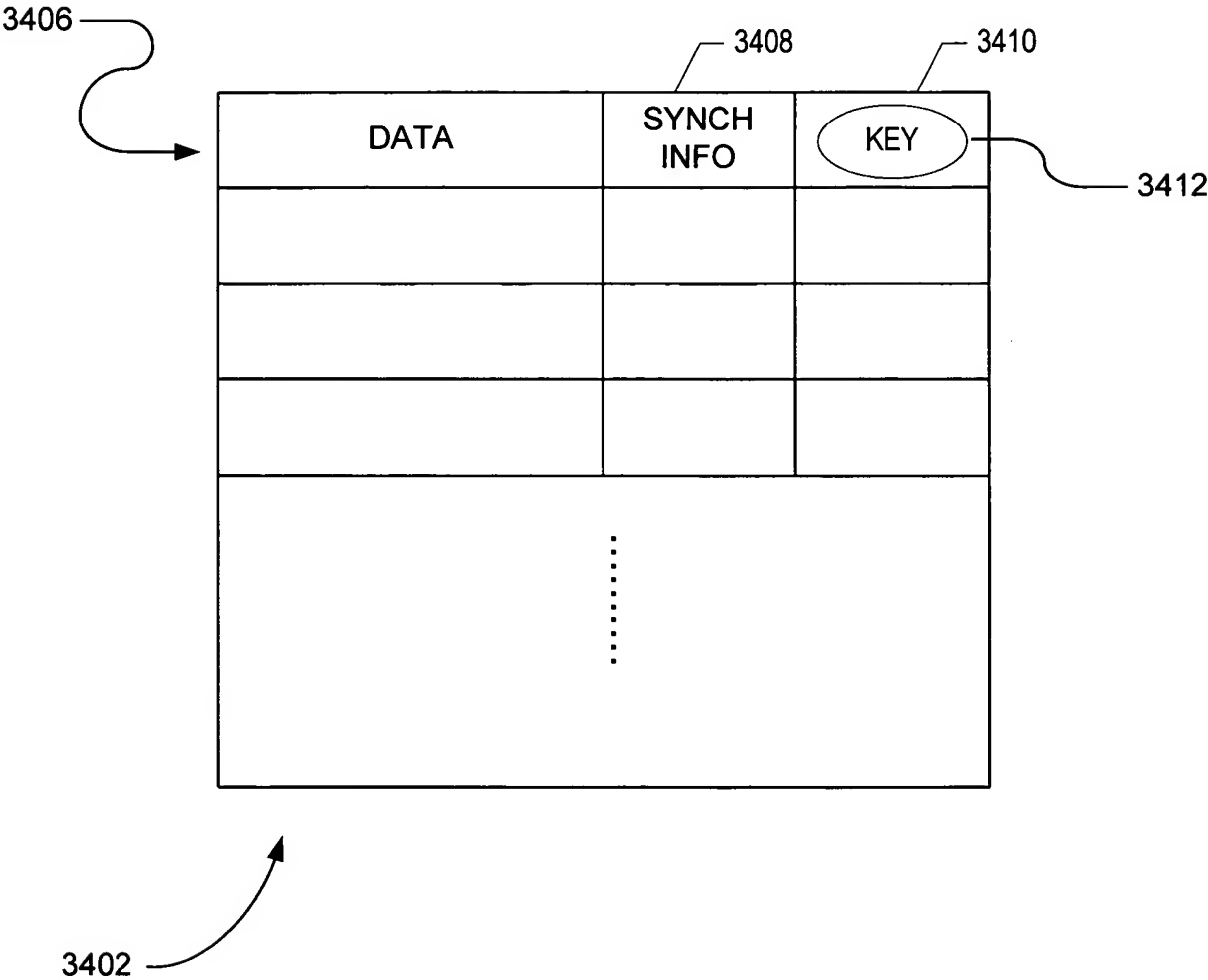


Figure 34

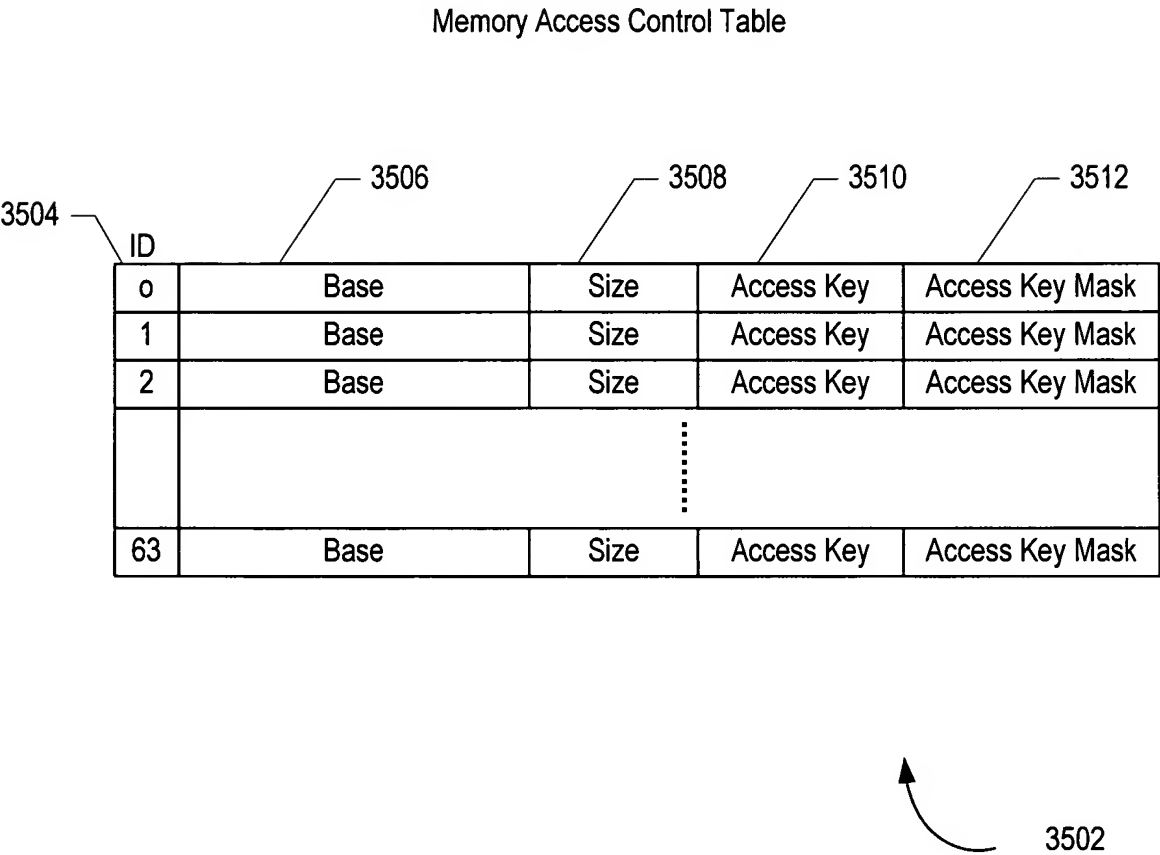
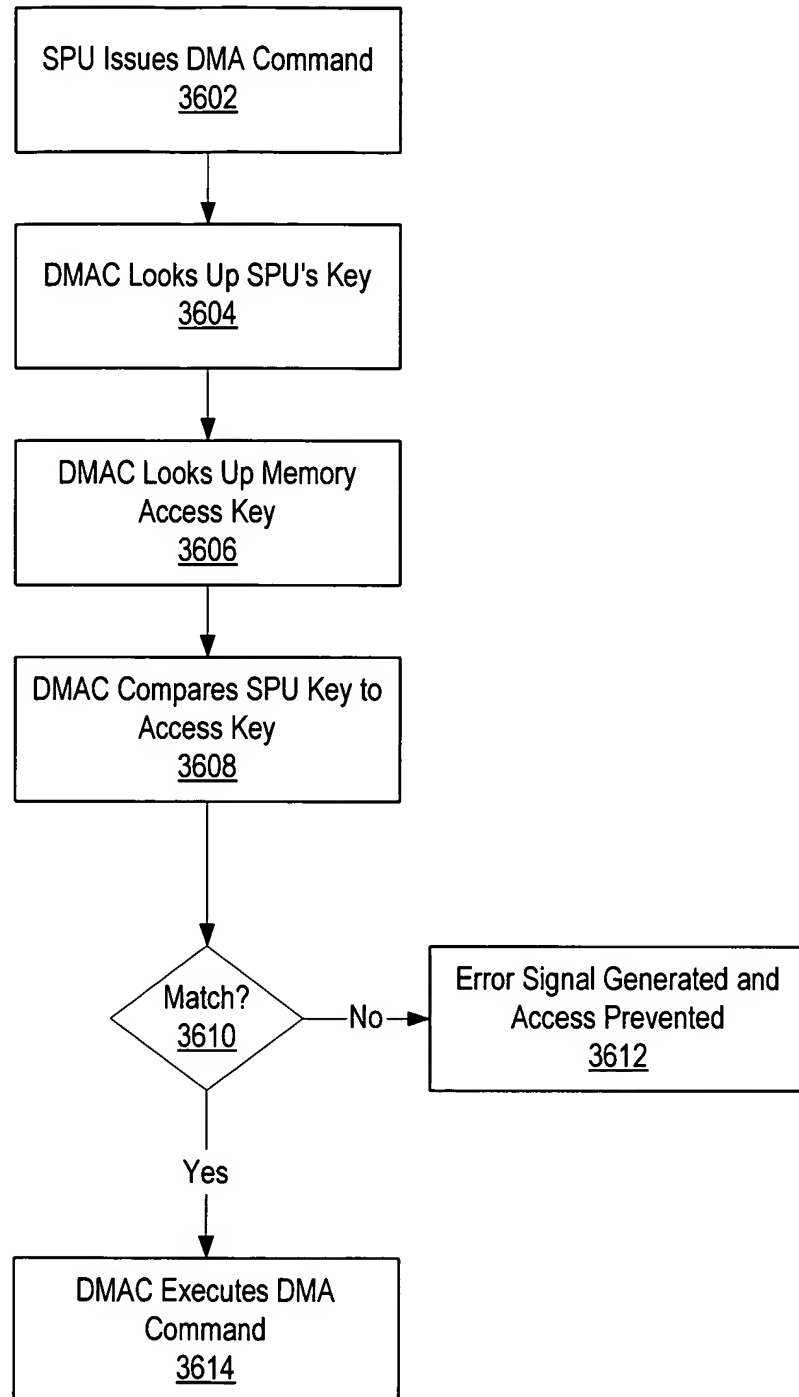
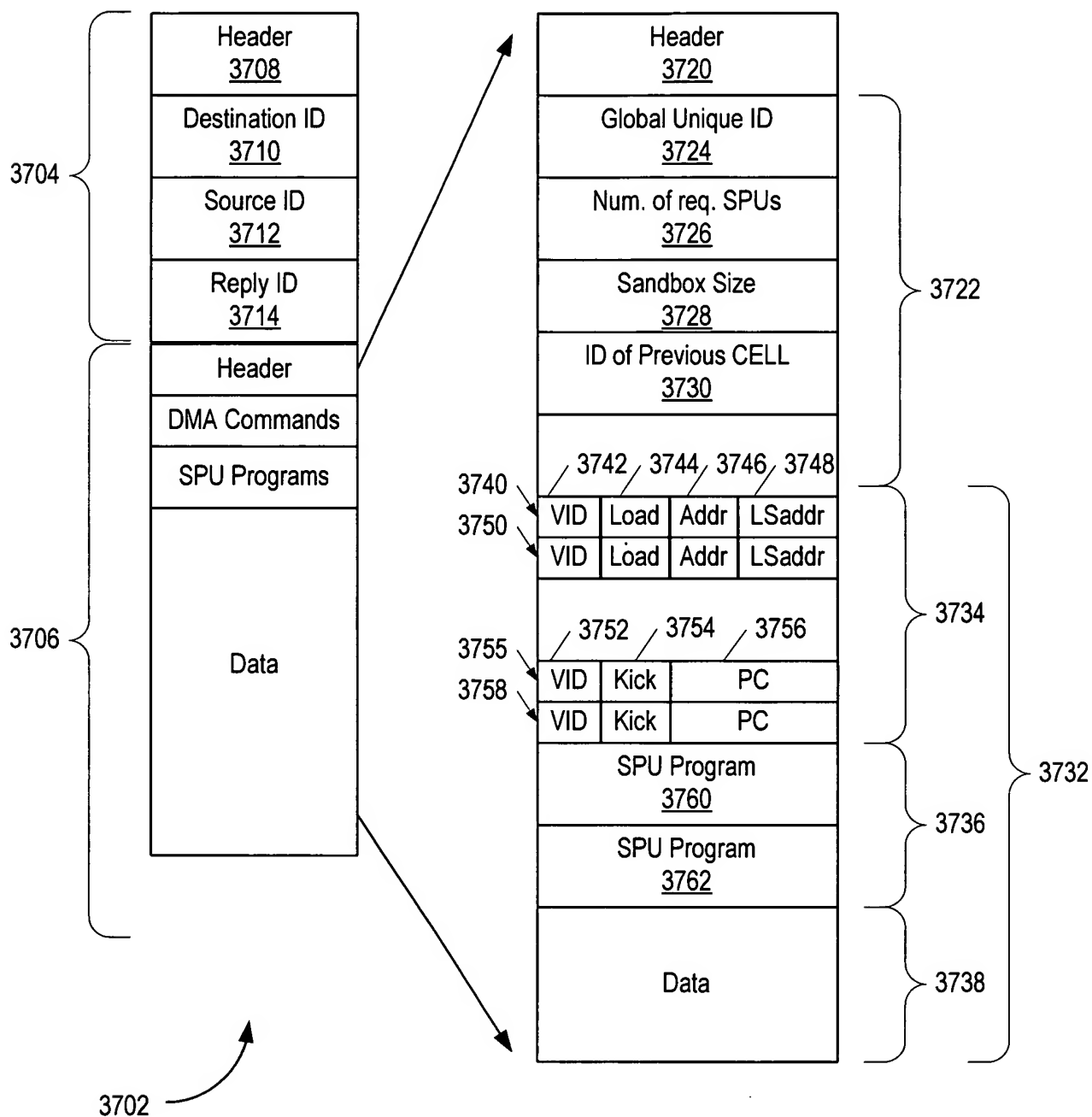


Figure 35

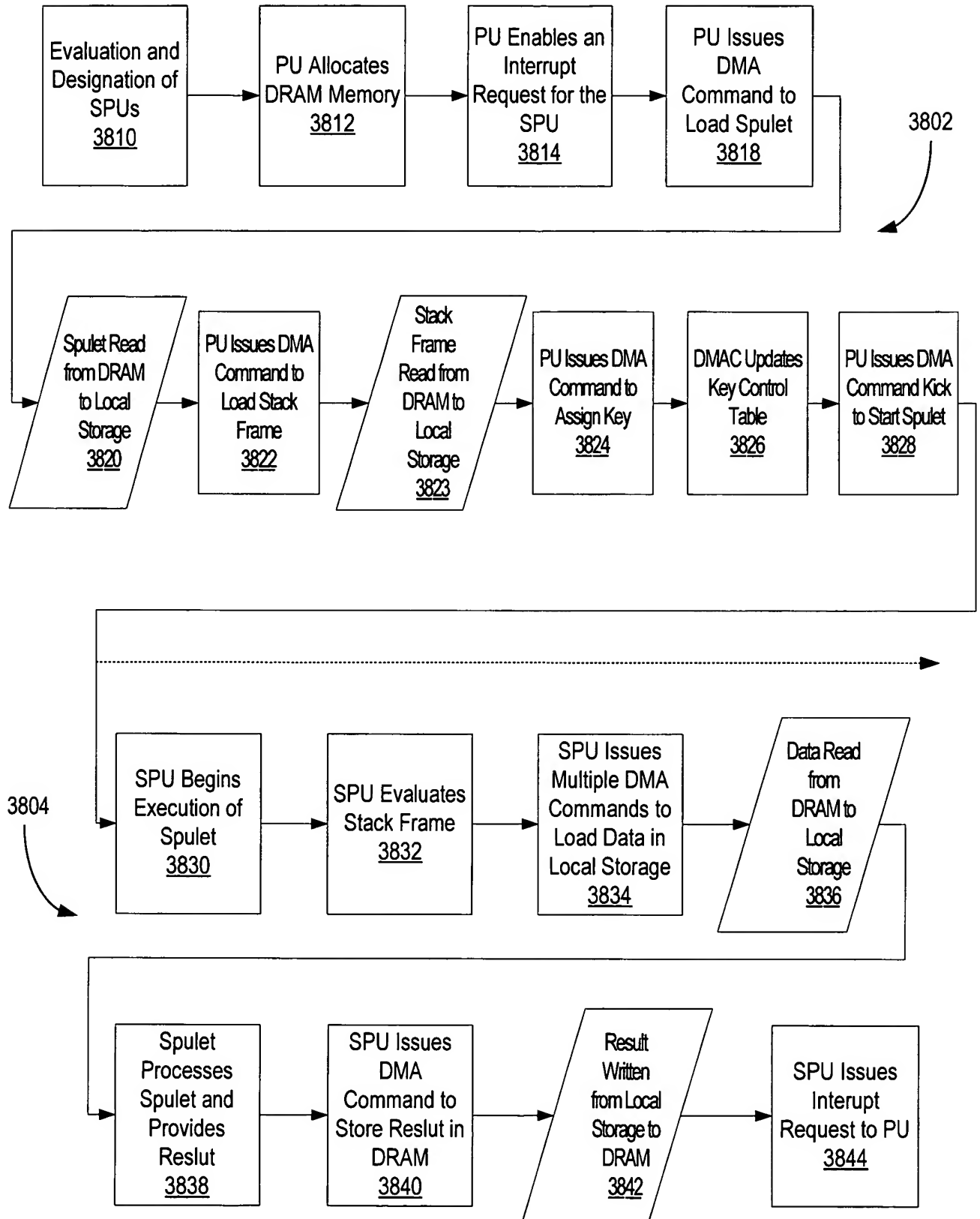
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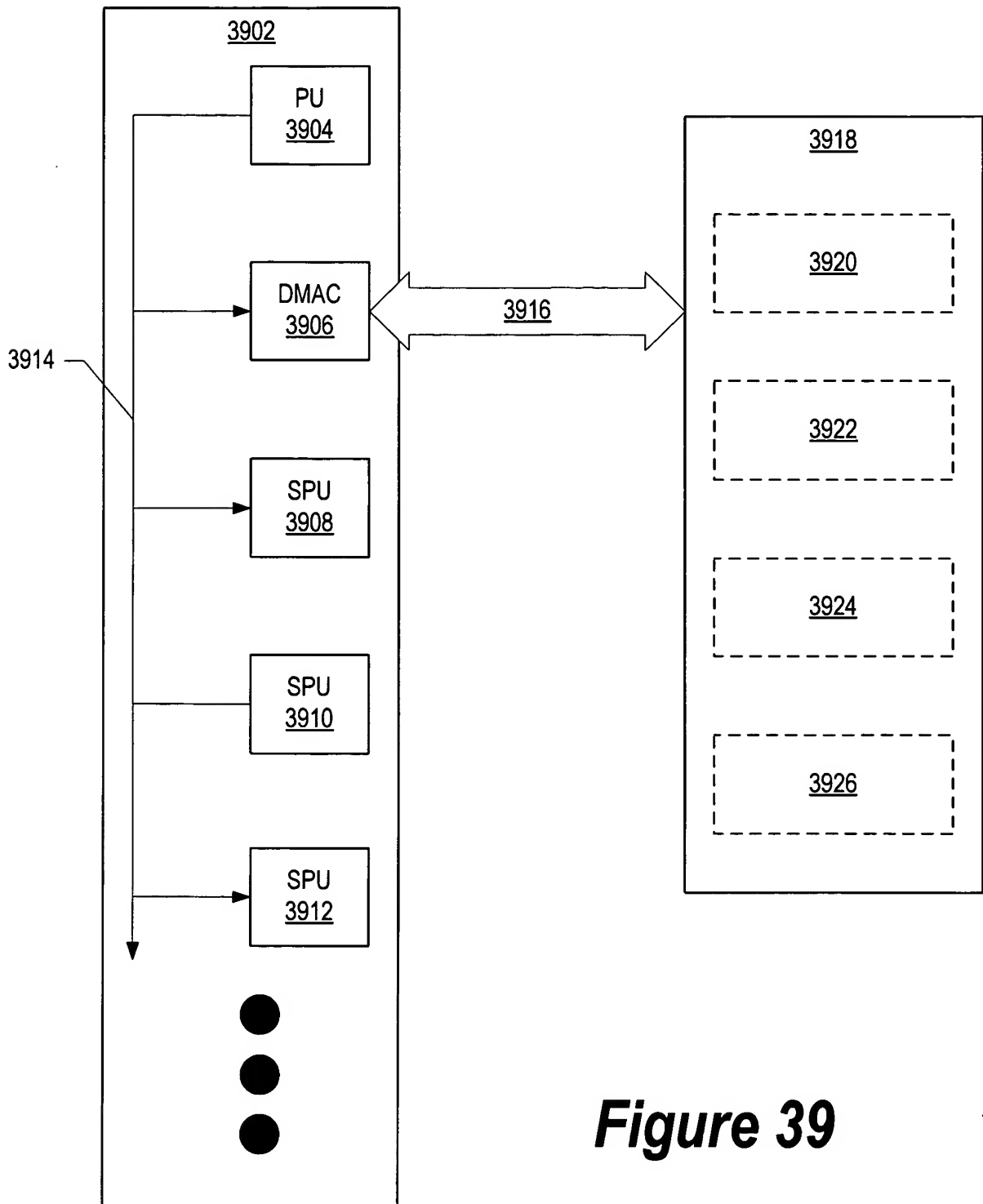
**Figure 36**

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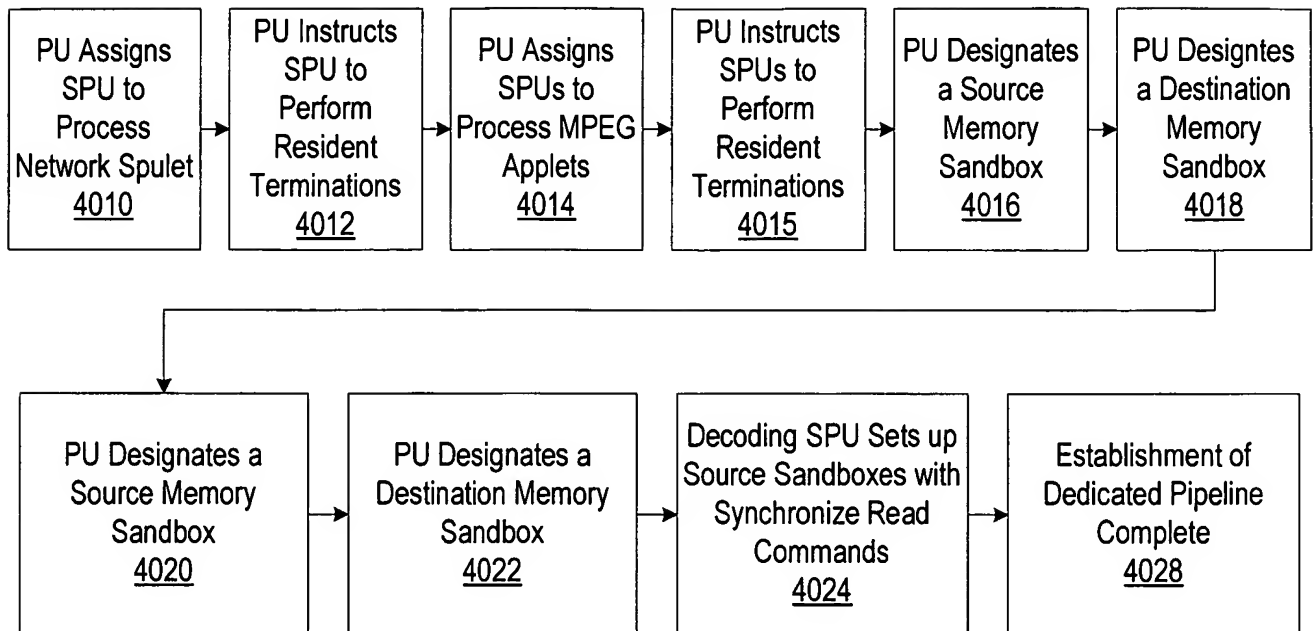
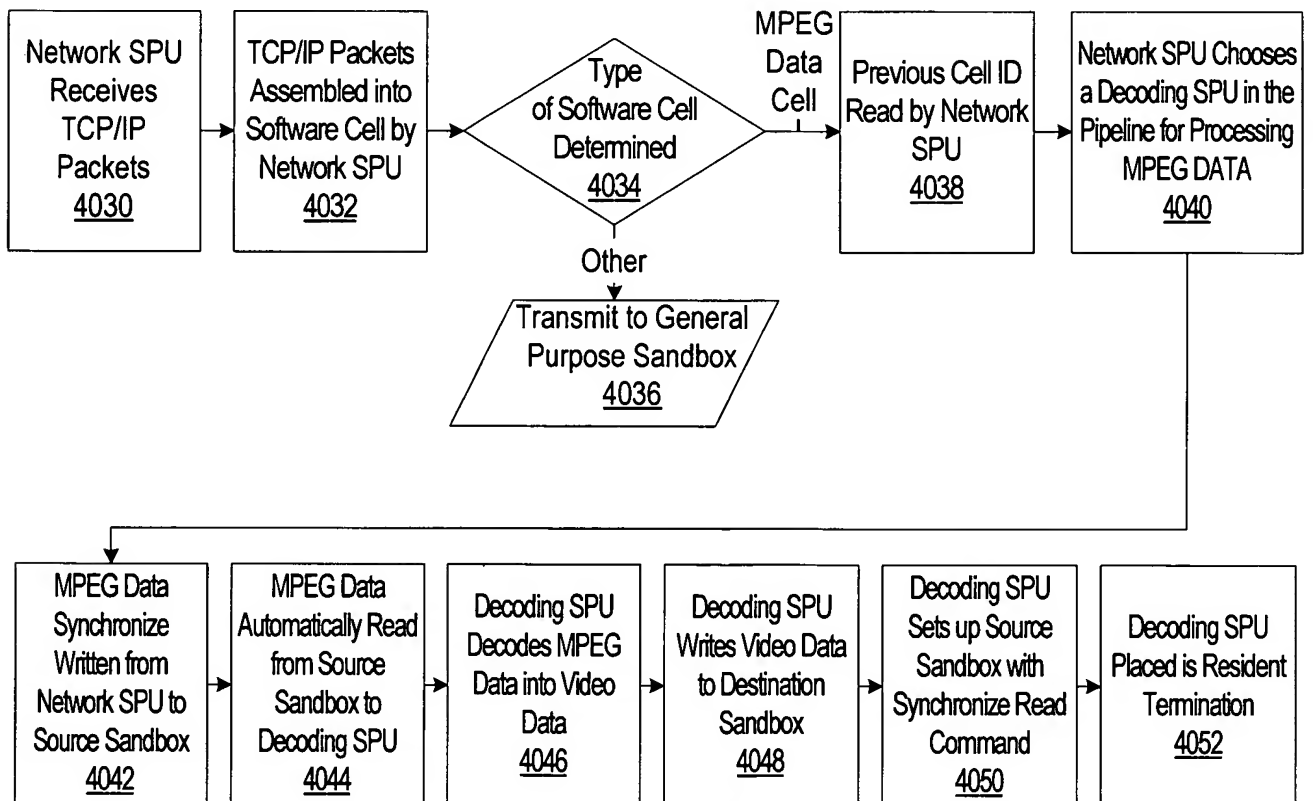
**Figure 37**

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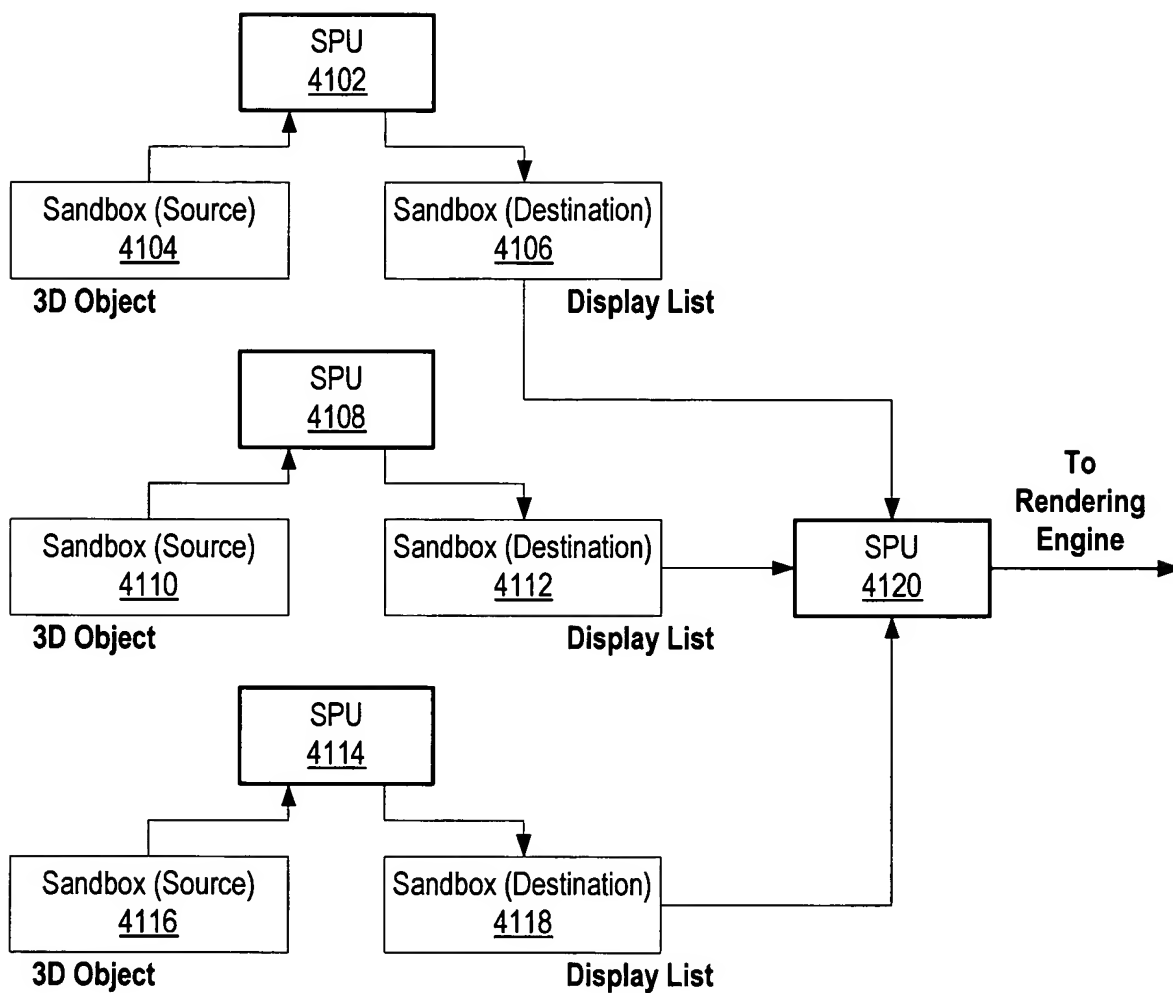
**Figure 38**

**Figure 39**

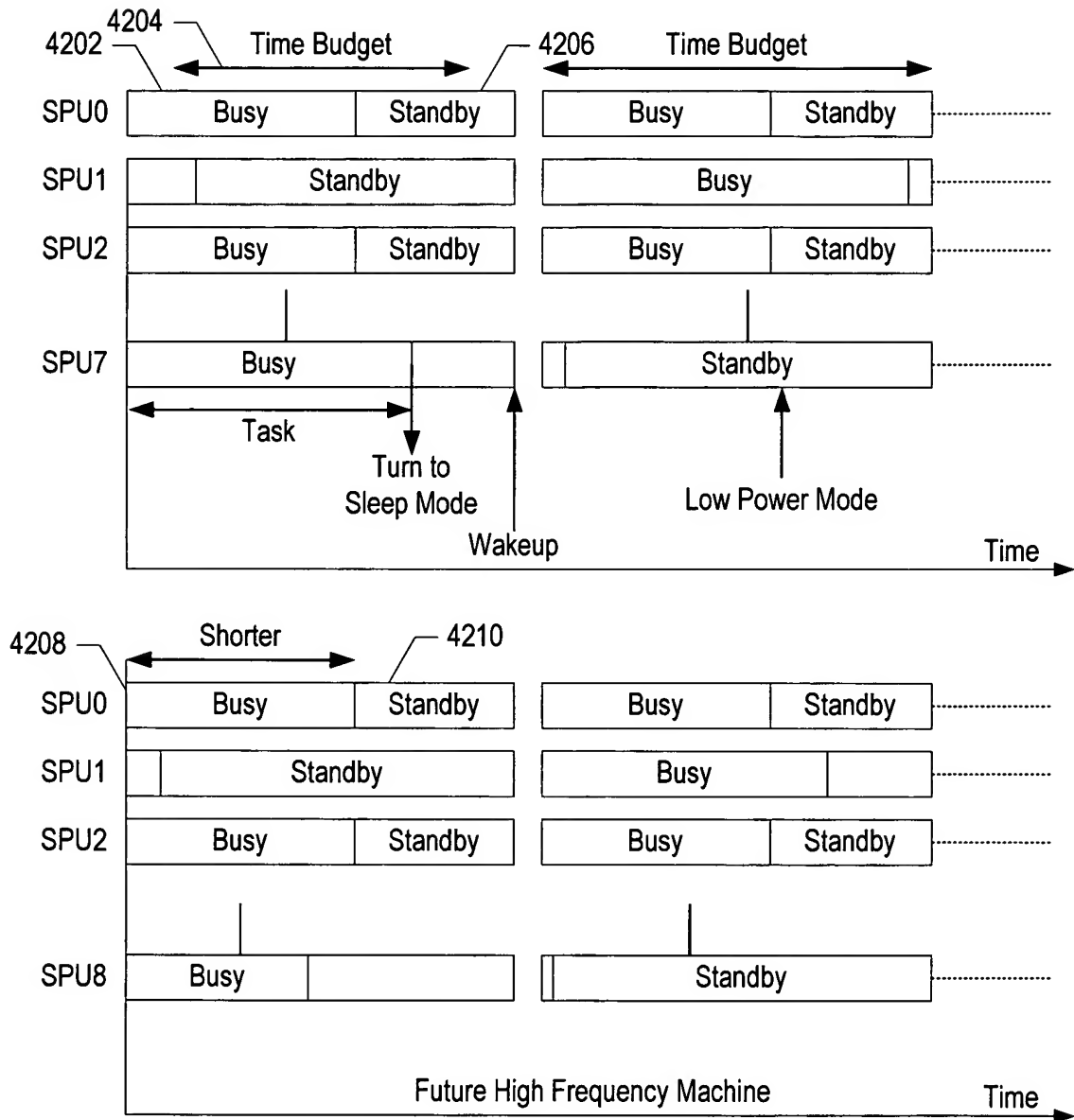
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**Figure 40A****Figure 40B**

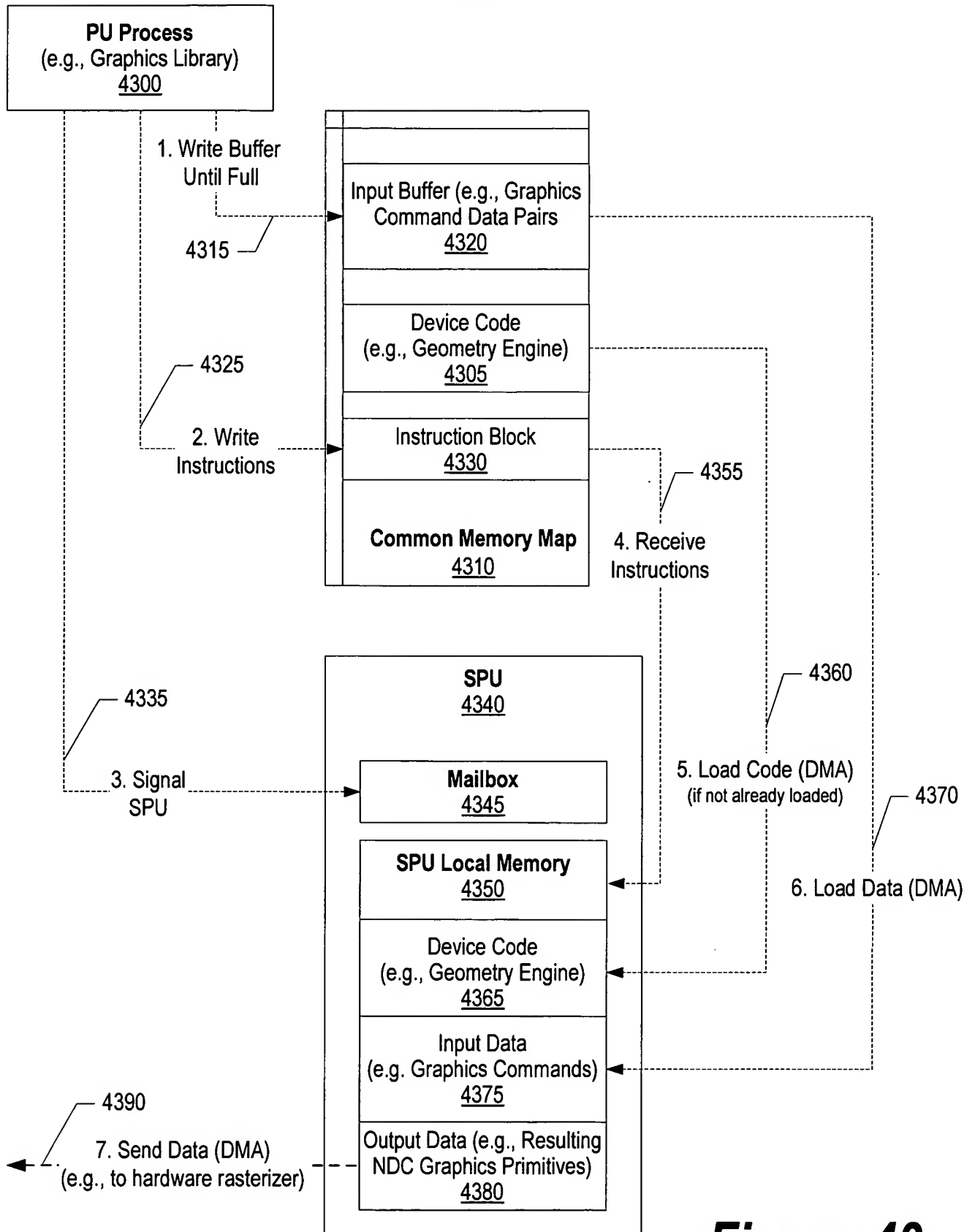
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**Figure 41**

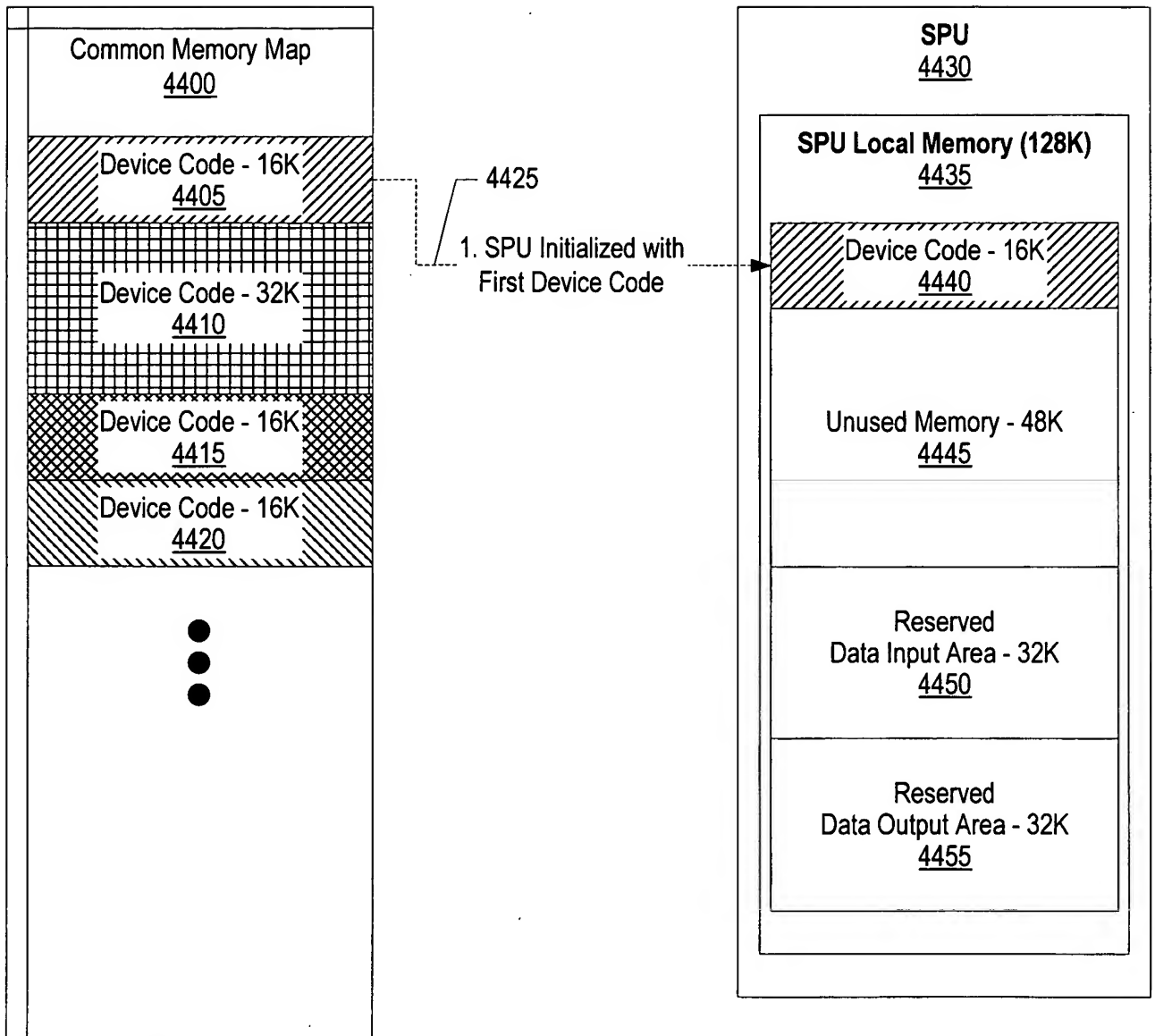
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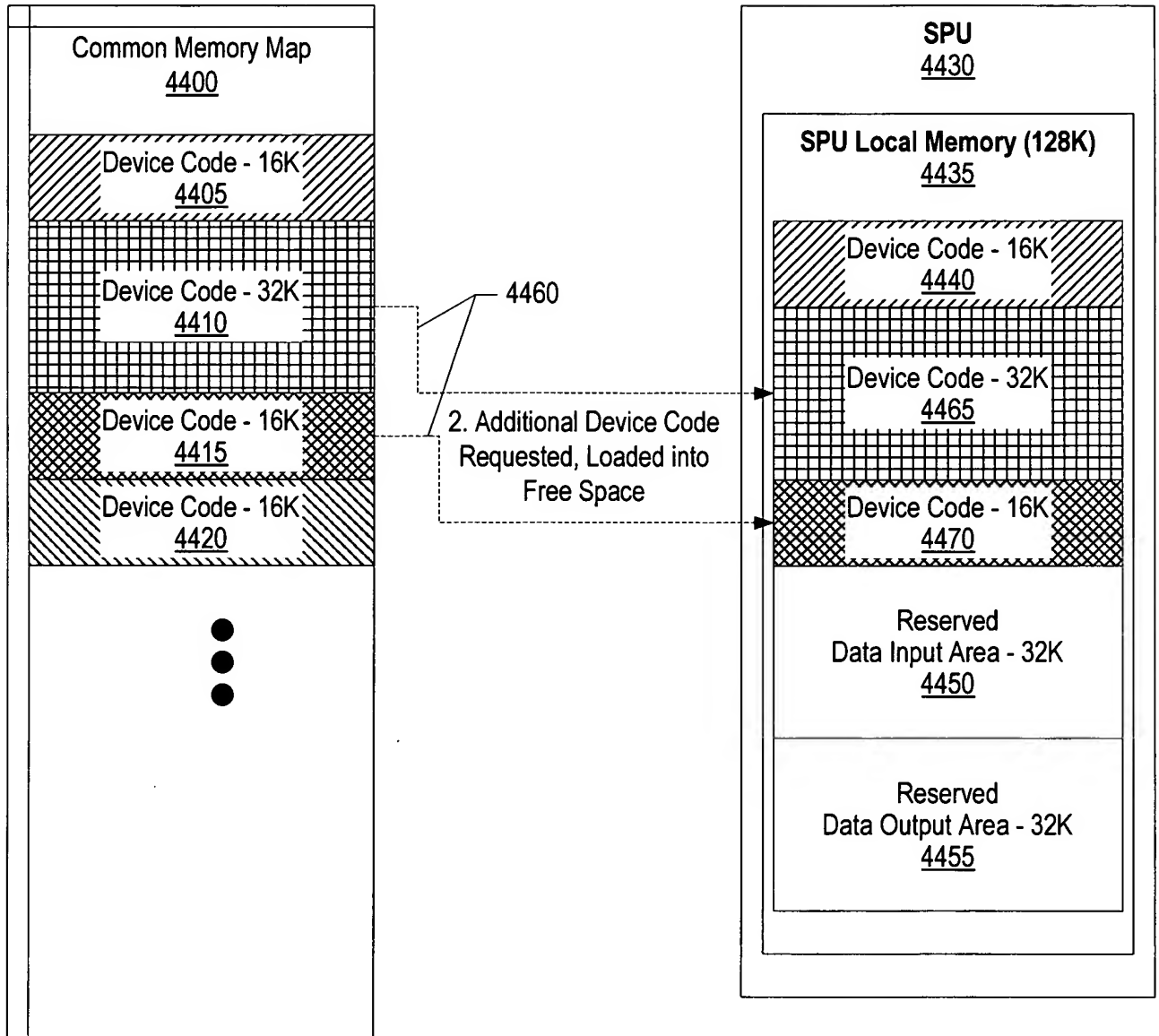
**Figure 42**

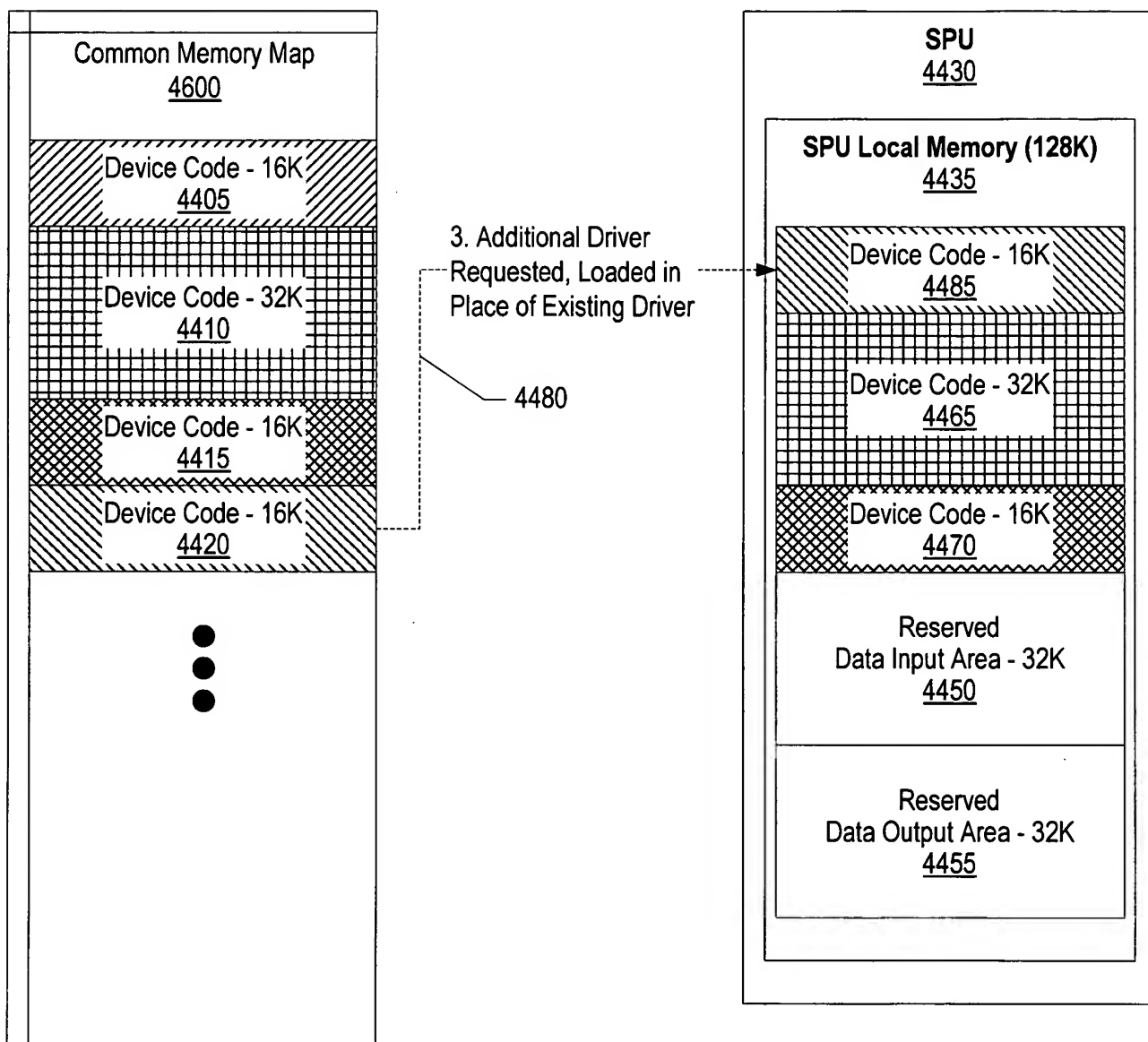
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**Figure 43**

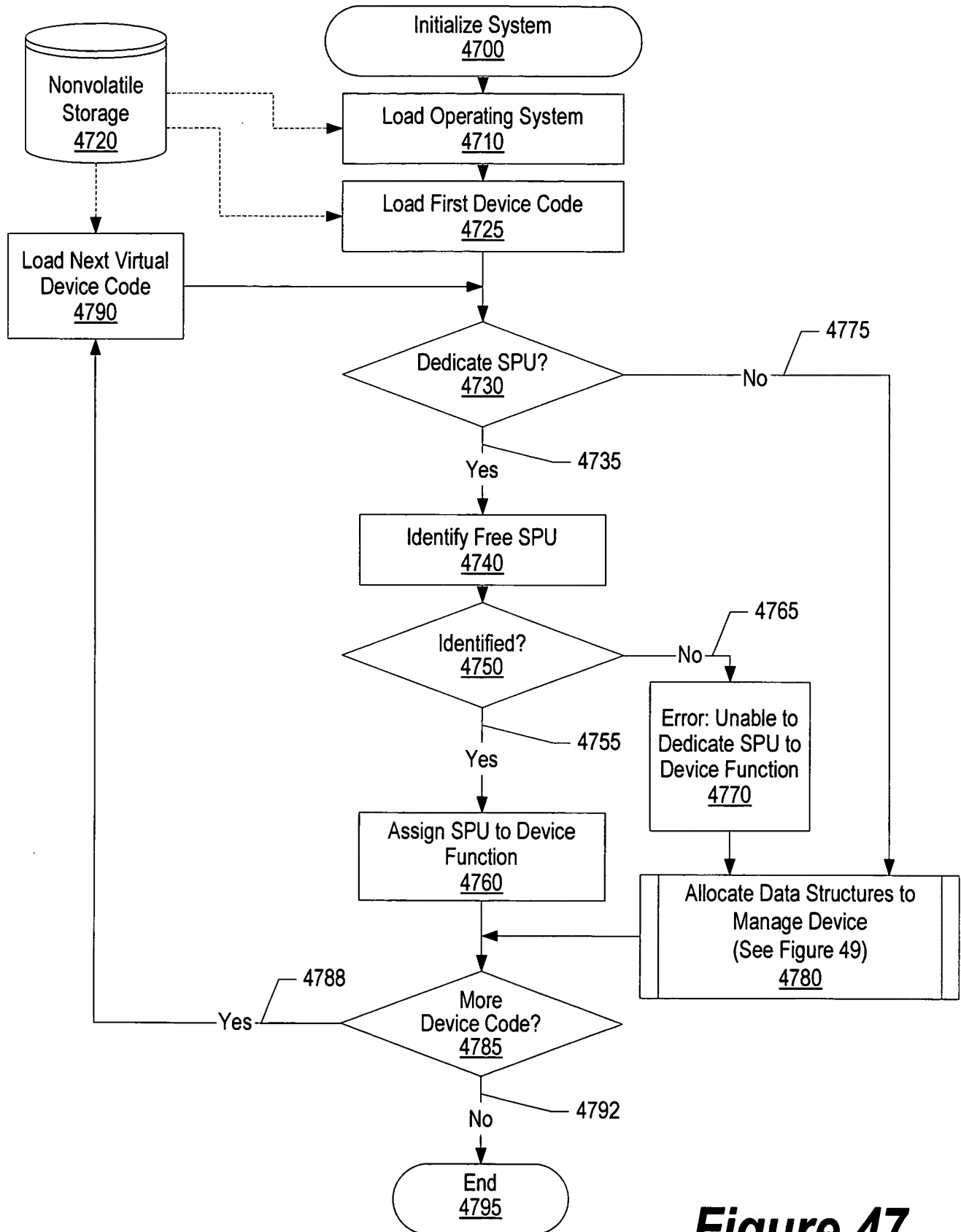
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**Figure 44**

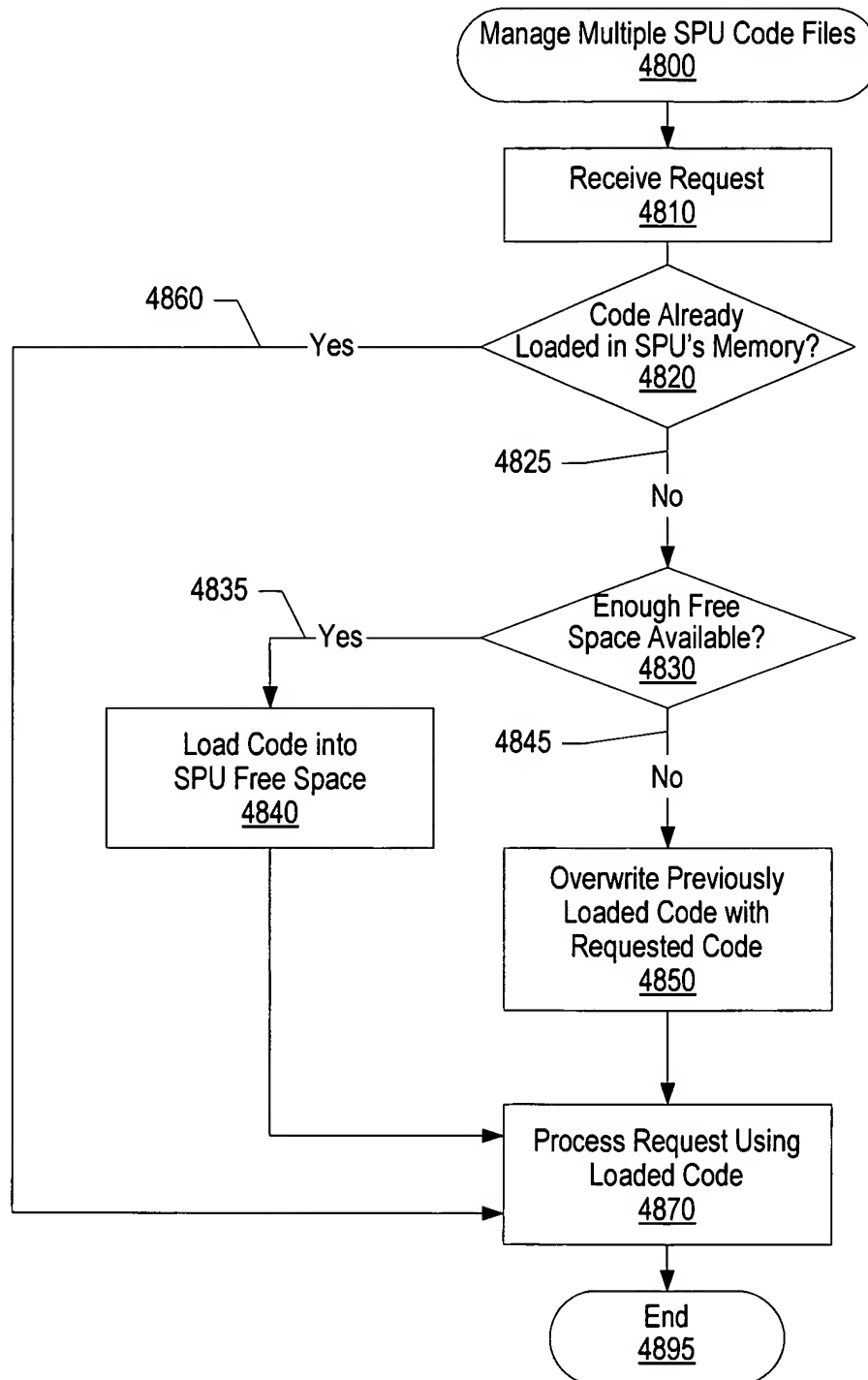
**Figure 45**

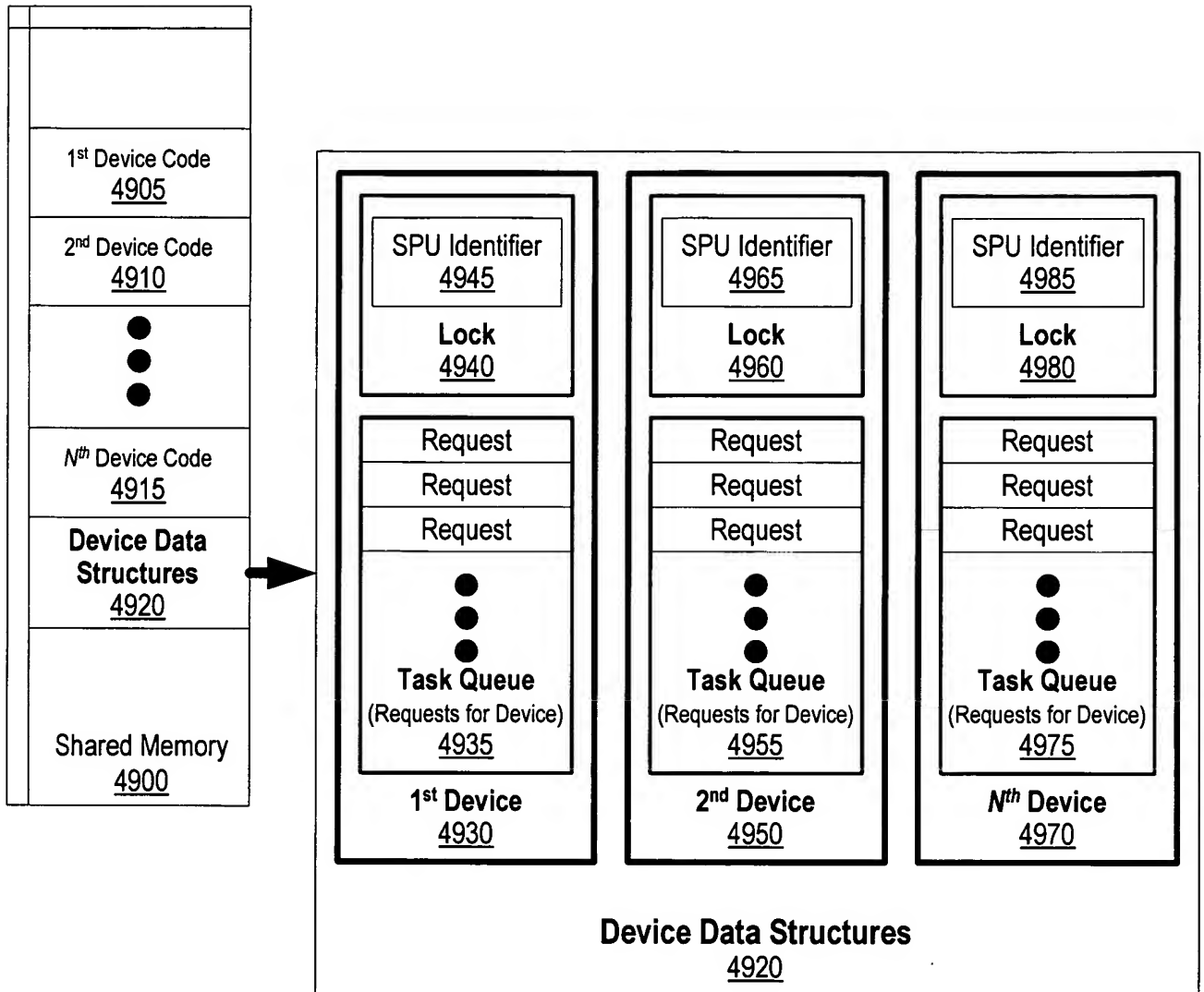
**Figure 46**

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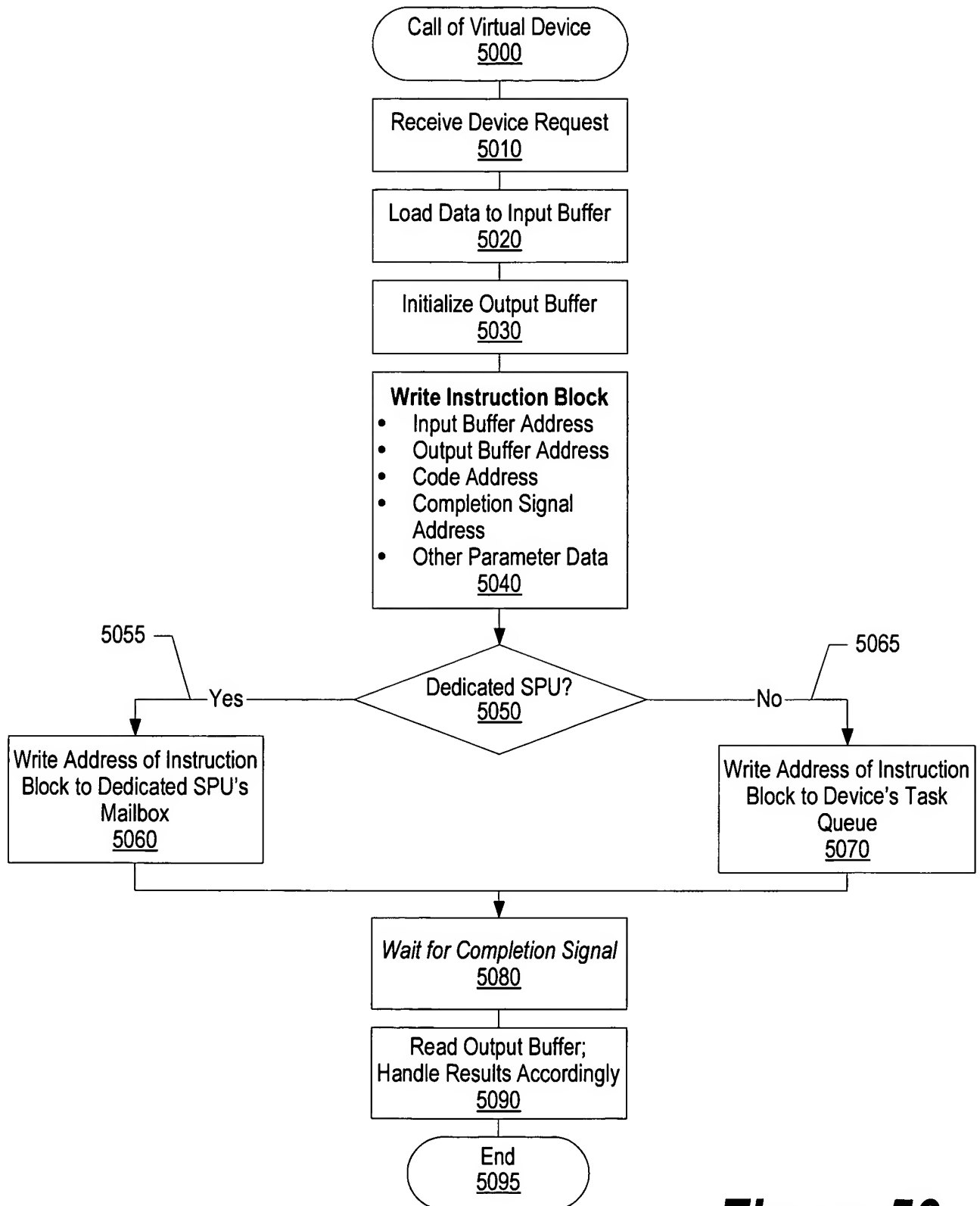
**Figure 47**

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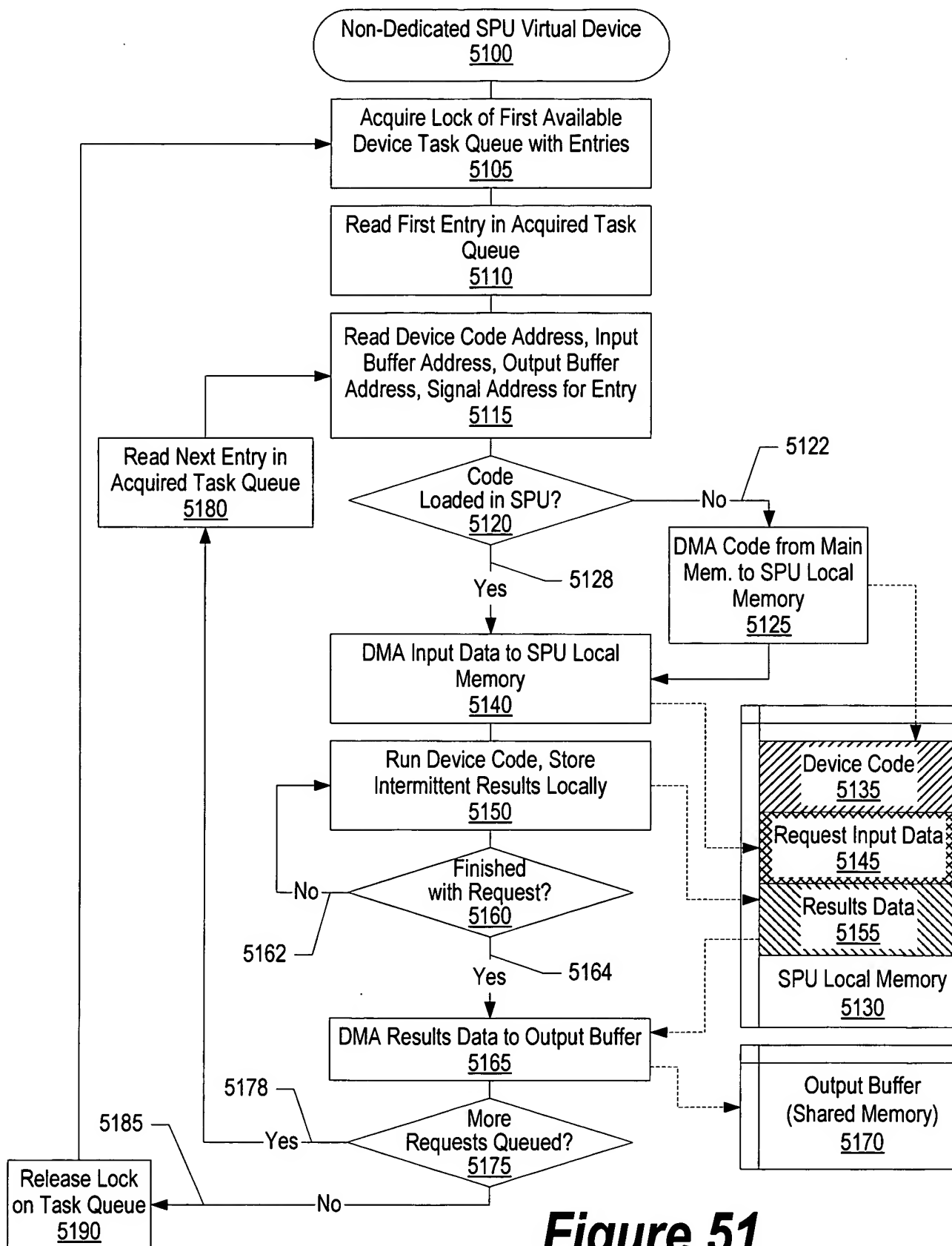
**Figure 48**

**Figure 49**

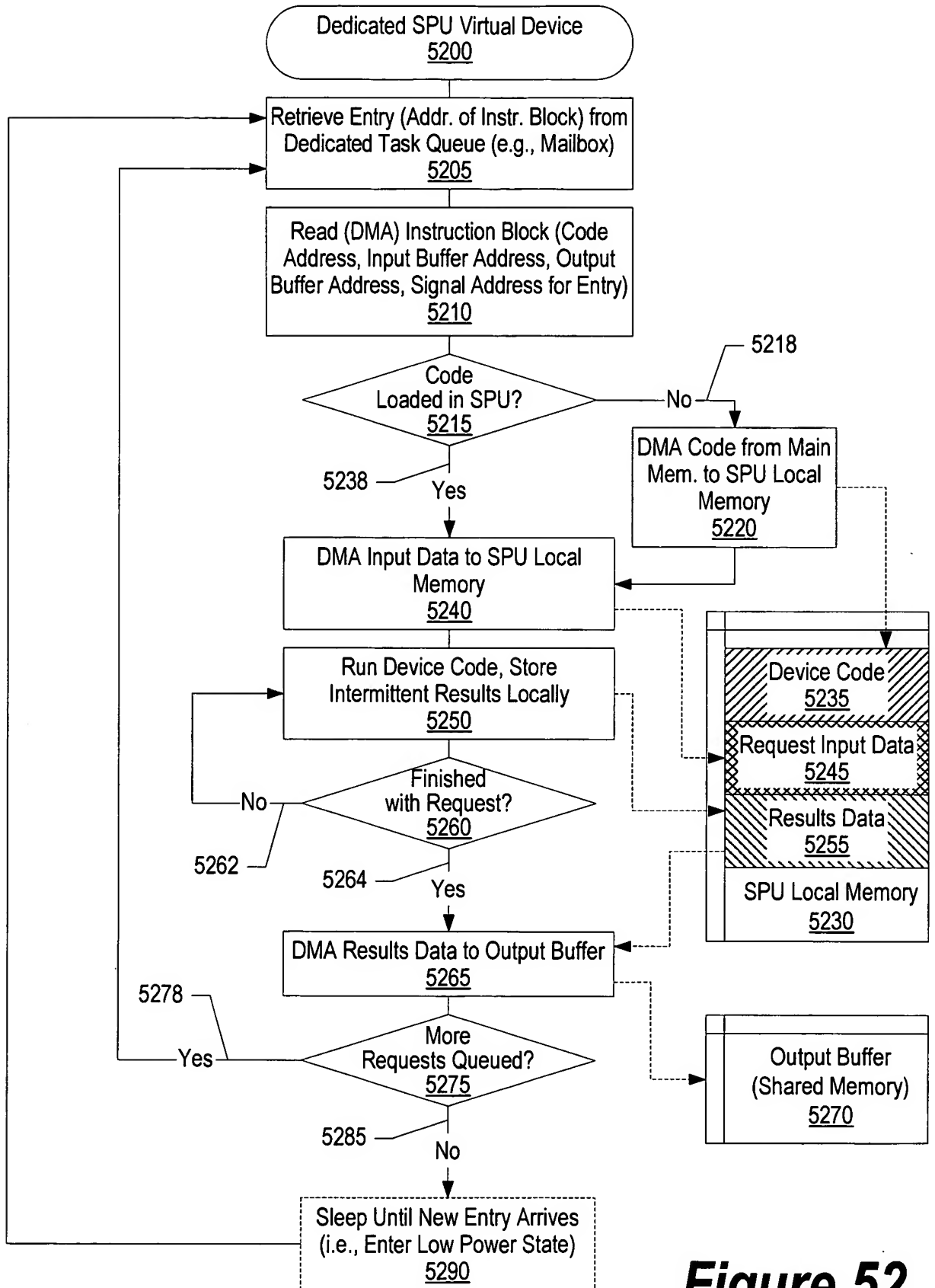
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**Figure 50**

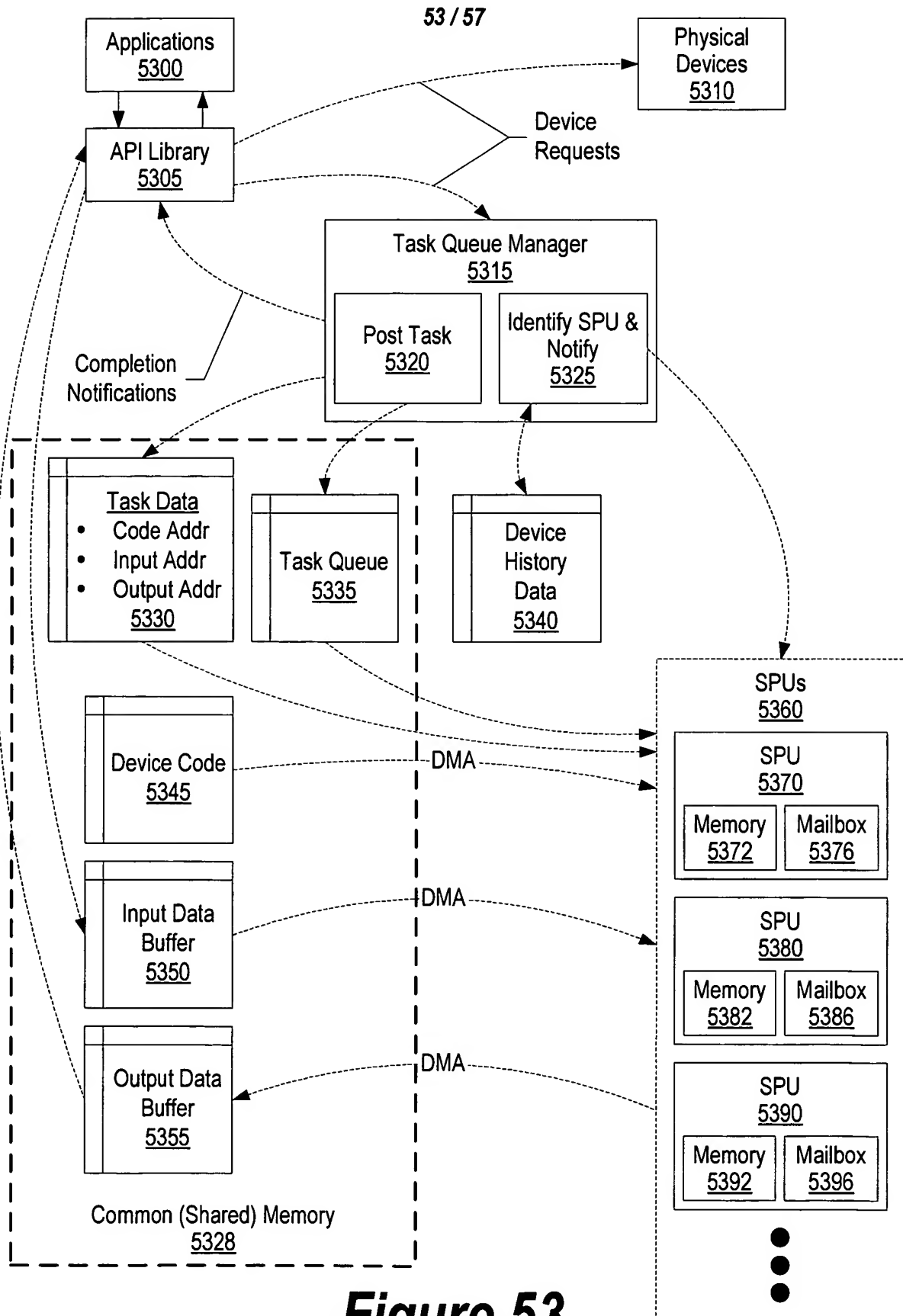
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**Figure 51**

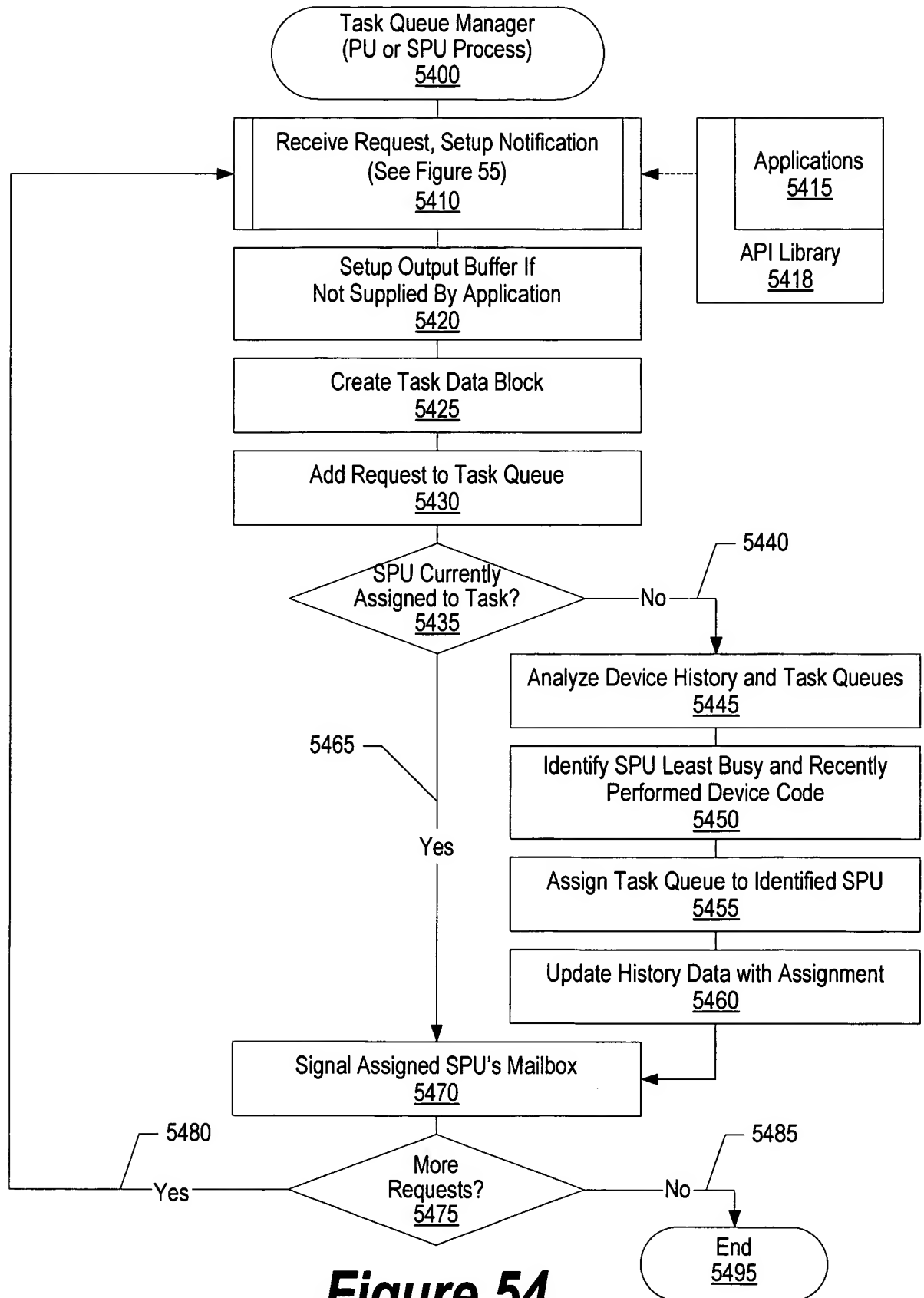
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**Figure 52**

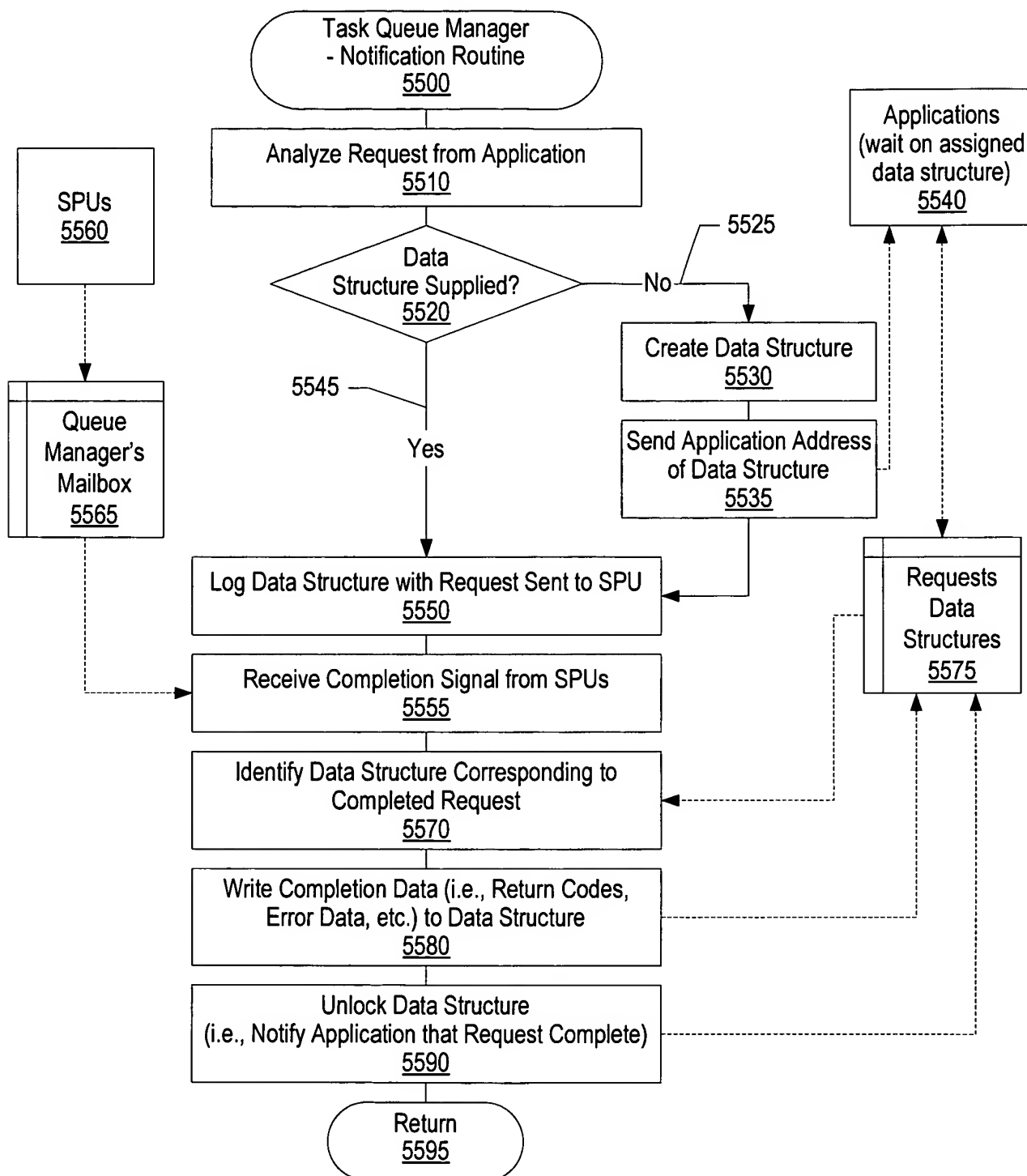
System and Method for Virtual Devices Using a Plurality of Processors

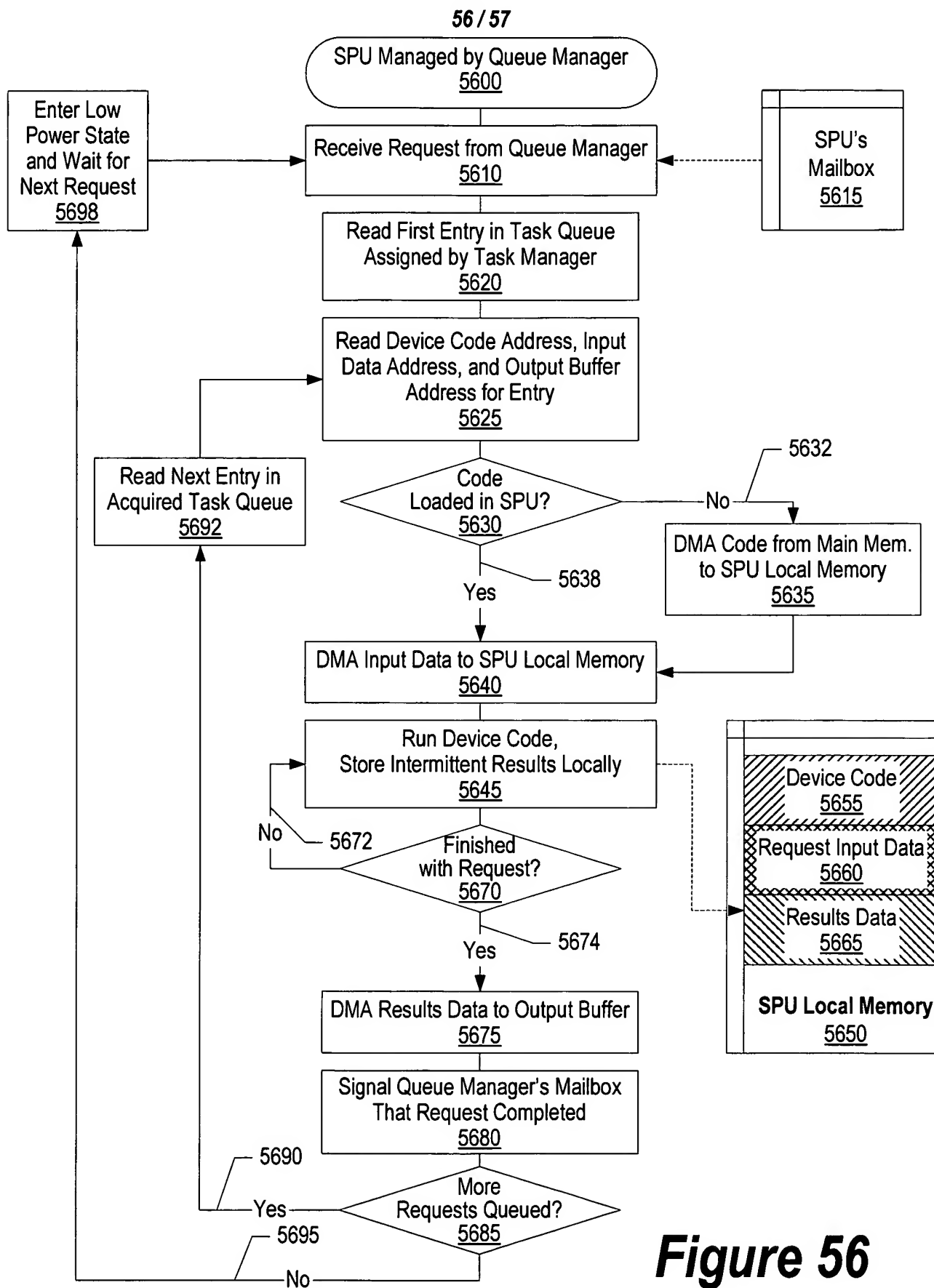
**Figure 53**

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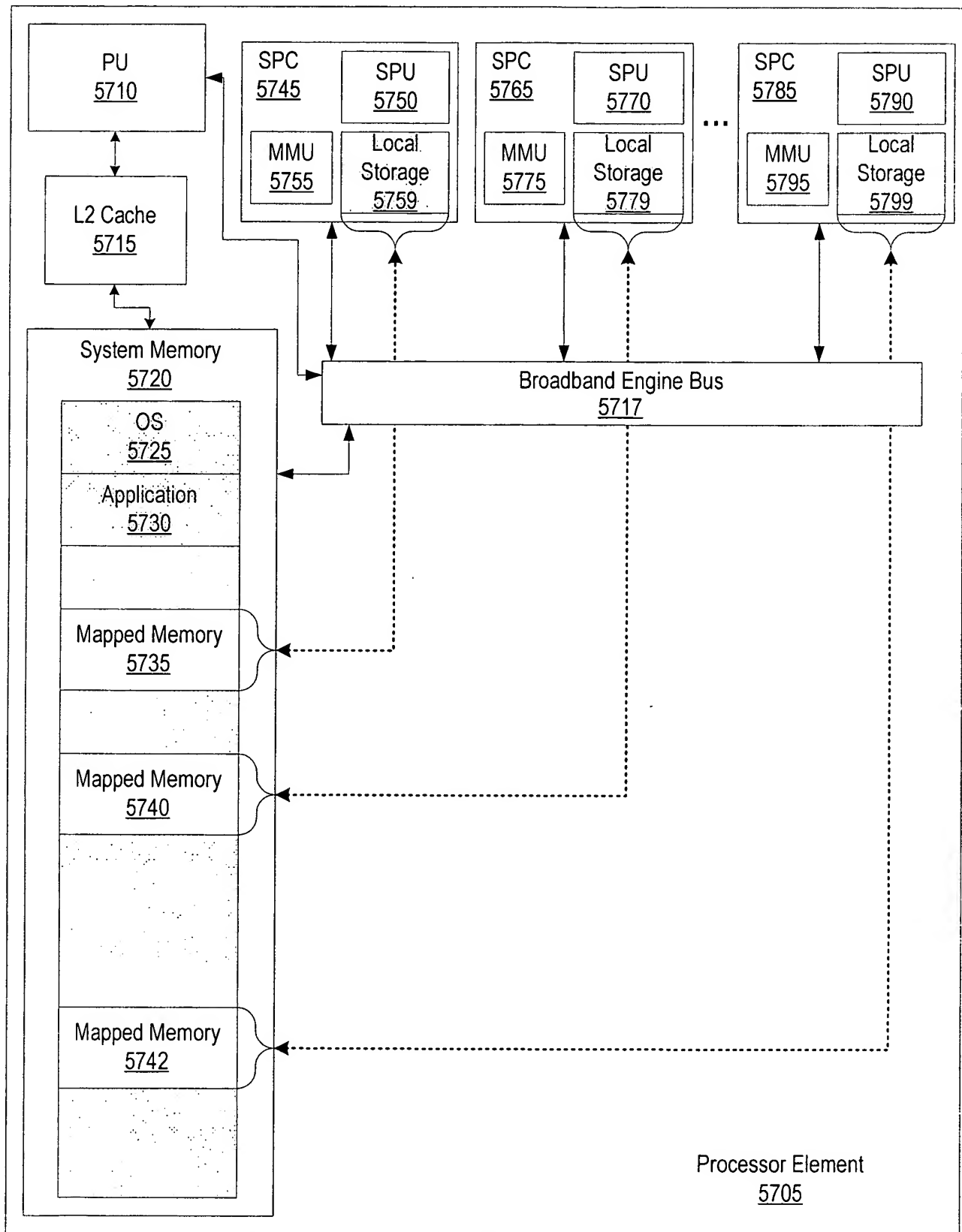
**Figure 54**

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**Figure 55**



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**Figure 57**